NGCAS 2018

The 2nd New Generation of Circuits and Systems Conference

Conference Guide

20th November 2018
University of Malta Valletta Campus

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Welcome Message

On behalf of the Organising Committee it is my pleasure to welcome you to Malta and the 2nd New Generation of Circuits and Systems Conference, being held at the University of Malta Valletta Campus on 20th November 2018.

I would like to thank all those who have made NGCAS 2018 possible. First of all the authors who have come here from all over the world to present the results of their scientific and technical research. Such a Conference is only possible because of the hard work, dedication and time-consuming activities carried out beforehand. The Technical Program Committee and the Track Chairs have prepared a truly excellent technical program and together with the reviewers selected in a short time the 51 papers being presented at NGCAS 2018 in regular lecture and poster sessions. NGCAS 2018 also features an invited Plenary Session from the industry. I would like to thank both the organisers and the speakers at all of these sessions.

It is now time to wish you a memorable experience in Malta. I encourage you to not only renew your acquaintances during the conference but also to meet new actors in your field, promoting and supporting the participation of the more junior staff and research students. I also encourage you to enjoy the hospitality of Malta and to sample its long history and culture.

Edward Gatt
General Chair, NGCAS 2018

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NGCAS 2018 Programme

Monday 19th November 2018

18:00-19:00	Registration
19:00-20:30	Welcome Reception

Tuesday 20th November 2018

08:00-09:00	Registration
09:00-09:15	Opening Ceremony
09:15-10:15	Keynote Presentation
10:15-10:45	Coffee Break
10:45-11:15	***A1P-C:*** Poster Session 1 Short Presentations *(Auditorium – Level 2)*
11:15-12:45	Parallel Sessions
	A1P-C: *Poster Session 1* *(Poster Area – Level 2)*
	A1L-A: *Analog Circuits and Systems* *(Auditorium – Level 2)*
	A1L-B: *Digital Circuits and Systems* *(Room 3 – Level 1)*

12:45-13:45 Lunch Break

13:45-14:15 ***A2P-C:*** Poster Session 2
Short Presentations
(Auditorium – Level 2)

14:15-15:45 Parallel Sessions

A2P-C: *Poster Session 2*
(Poster Area – Level 2)

A2L-A: *CAD and Electronic Design Automation*
(Auditorium – Level 2)

A2L-B: *Nonlinear Systems and Applications*
(Room 3 – Level 1)

15:45-16:15 Coffee Break

16:15-18:00 Parallel Sessions

A3L-A: Circuits & Systems for Communications
(Auditorium – Level 2)

A3L-B: VLSI Systems & Applications
(Room 3 – Level 1)

19:00-23:00 Social Event
Walking Tour of Imdina & Dinner

Keynote Speaker

Professor JOSEPH CILIA
B. Elec. Eng. MSc. PhD.

Professor Joseph Cilia obtained his first degree in electrical engineering in 1989 from the University of Malta, under the worker student scheme. After 3 years work experience at the local power station he won a scholarship to read a master degree on the same subject at the University of Nottingham. Based on his experience and performance during his master degree, Nottingham University awarded him a scholarship to proceed with his Phd studies. His studies were sponsored by a consortium of 5 UK companies to carry out industrial research on sensorless vector control of induction motors. His work was presented in international conferences and patented. Professor Cilia is a lecturer at the University of Malta on the theory and design of electric drive systems. In 2003 he was appointed as C.E.O and Research Director of Abertax Group and in 2010 the Chairman of Abertax executive board. He has also served as Deputy Chairman of the Malta Resources Authority and currently the Chairman of the National Skill Council. In 2009 he was also appointed a Member of Eurobat where he has been involved in a number of white papers published on his field of expertise. Professor Cilia has 16 international patents and has published over 100 papers in international conferences and his research interests are on high speed drive systems, electrical transport, energy storage systems, efficient use of energy and renewables. His main goal is to educate, help and guide, students and employees, to create added value manufacturing through innovation.

Abstracts

A1L-A: Analog Circuits and Systems

Session Type: Lecture
Location: Auditorium (Level 2)

A Bit Cycling Method for Improving the DNL/INL in Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)
Hua Fan, Chen Wang, Quanyuan Feng, Dagang Li, Xiaopeng Diao, Lishuang Lin, Hadi Heidari

This paper presents a bit cycling method to improve the max root mean square (rms) value of differential nonlinearity (DNL) and the max rms value of integral nonlinearity (INL) for successive approximation register (SAR) analog-to-digital converter (ADC). Neither an additional DAC nor any complex correction algorithm are needed in this work, it is only necessary to switch between two different bit cycling modes, then it is possible to avoid the accumulation error of the capacitor mismatch caused by the same codes, so as to achieve the purpose of upgrading DNL and INL, and finally to improve the static linearity of SAR ADC.

Variable Transconductance Voltage Differencing Current Coveyor and its Application in Filter Design
Suyash Kumar, Gunit Dhingra, Pragati Kumar

This paper proposes a novel design of variable transconductance voltage differencing current conveyor (VT-VDCC). The proposed design provides for increased tunability range of the transconductance of the VT-VDCC resulting in wide tuning range with low power dissipation. The performance of the proposed VT-VDCC has been verified by designing a current-mode universal filter. Workability of the designed circuit has been established with PSPICE simulations using TSMC 0.18 μm CMOS process parameters.

Versatile SAR-ADC for Biomedical Applications
Julien Sotiere, Mehdi Terosiet, Edwin De Roux, Alejandro Von Chong, Florian Kolbl, Aymeric Histace, Olivier Romain

This paper presents a versatile SAR ADC targeting the acquisition of signals in biomedical applications. The converter is implemented in a CMOS AMS 0.35 μm technology and powered with 3.3 V. Its output bit-width can be varied from 4 to 8 bits. The device includes built-in programmable clock generator and voltage reference circuit. The sampling rate can be tuned up to 100 kS/s in the 8-bit mode and with a maximal input range of 2.5 V. All these parameters can be independently adjusted. This is a unique fully-configurable converter. The simulation results are reported and positioned with respect to the most recent designs.

Impact of the Spread-Spectrum Technique on the Higher-Order Harmonics and Radiated Emissions of a Synchronous Buck Converter
Raul Blecic, Fabio Pareschi, Josip Bacmaga, Riccardo Rovatti, Gianluca Setti, Adrijan Baric

Synchronous buck converters generate electromagnetic emissions which may violate the limits specified in the regulations. Spread-spectrum is an effective technique for reducing the electromagnetic interference of switching devices. The reduction of the magnitude of the first harmonic by the spread-spectrum technique is mainly in focus in the literature. In this paper, the impact on the higher-order harmonics and on the radiated emissions is analyzed. A non-regulated synchronous buck converter is used as a device under test. The radiated emissions of the converter are calculated from the measurements performed by a transverse electromagnetic cell and a hybrid coupler. The measurements are performed for different values of the parameters of the spread-spectrum technique and a reduction of up to 5.7 dB is obtained.

Photodiode Bridge-Based Differential Readout Circuit for High-Sensitivity Measurements of Energy Variations of Laser Pulses for Optoelectronic Sensing Systems

Andrea De Marcellis, Elia Palange, Simona Leone, Guido Di Patrizio Stanchieri, Marco Faccio

In this paper we present an optoelectronic architecture based on a current-mode photodiode bridge readout circuit that performs differential measurements of the energy variations of nanosecond laser pulses. This operation is achieved by differentially detecting the currents photo generated by two Si photodiodes. The circuit can be optimised as a function of the laser pulse-width and of its repetition rate. The electronic circuitry allows to achieve the initial photodiode bridge balancing condition by means of variable control voltages. The readout circuit has been characterised by varying its gain, detection sensitivity and energy-per-pulse, employing 10 ns laser pulses at 20 Hz. These measurements have been compared with those ones obtained using a standard commercial lock-in amplifier as the conditioning circuit under the same experimental conditions. The proposed optoelectronic architecture is able to reach a maximum detection sensitivity of 7 mV/fJ corresponding to a detection resolution of the laser pulse energy variations equal to 0.14×10^{-3} fJ. These results prove an increase of 1225 of the sensitivity and resolution obtained by employing a commercial lock-in amplifier.

A1L-B: Digital Circuits and Systems

Session Type: Lecture
Location: Room 3 (Level 1)

Correlating Power Efficiency and Lifetime to Programming Strategies in RRAM-Based FPGAs
Cristian Zambelli, Marco Castellari, Piero Olivo, Davide Bertozzi

There is currently a surge of interest in RRAM based FPGAs because of their lower area, power loss resilience and their suitability for near-threshold operation. However, materializing lower dynamic and static power dissipation turns out to be challenging, since this depends on the capability of the technology to infer a large separation between RRAM resistance states. While programming strategies have been developed to achieve this, their side effects in terms of programming power overhead and lifetime of RRAM cells are typically overlooked. The justification brought by previous work consists of the typically-low number of runtime reconfigurations of FPGA devices. This paper intends to pave the way for new usage models of RRAM based FPGAs, featuring augmented flexibility and dynamicity, thus lending themselves to emerging energy and workload-adaptive computing systems. The paper thus captures and quantifies the fundamental correlation between programming power of RRAM cells, operational static and dynamic power of mapped designs on FPGA, and device lifetime.

Efficient Implementation of Bi-Functional RTL Components - Case Study
Jan Nevoral, Richard Růžička

The emergence of highly optimized implementations of many bi-functional gates allows an efficient implementation of components at a higher level of abstraction. In several classes of applications which typically involve RT level oriented design approach, these components can circumvent various issues related to synthesis of multifunctional circuits at the gate level. While the synthesis at the gate level is difficult, at RT level a skilled designer is still able to design a far more complex circuits by

himself. If a set of efficient bi-functional RTL components is available, their utilization is expected to improve efficiency of the resulting circuit. In this paper, validity of this assumption is demonstrated through a design of bi-functional adder/subtractor circuit. At the gate level, one-bit full adder/subtractor circuit was created and optimised. This circuit was subsequently utilised for design of multi-bit adder/subtractor which was successfully simulated at the transistor level with MOSFET implementation of bi-functional logic gates. Besides adder/subtractor, an increment/decrement RTL component is also presented.

Smart Ultrasound Sensor for Non-Destructive Tests
Riccardo Matera, Valentino Meacci, Stefano Rossi, Dario Russo, Stefano Ricci, Didier Lootens

Ultrasounds plays a major role in Non-Destructive tests. An important application is the monitoring of the hardening process in cement-based materials. It was recently proven that ultrasound echoes reflected from the interface between a transmitting medium and the cement paste carry information about the status of the chemical process responsible of the cement hardening. In application like e.g. the monitoring of bridges or tunnels during construction, these sensors should be deployed in remote sites where they should work autonomously for days. Unfortunately, no electronics is currently available which satisfies the requirements for an industrial use. In this paper a completely configurable, embedded ultrasound system, capable of managing up to 8 ultrasound transducers, is presented. The proposed "smart" sensor can be remotely controlled through a web-based user-friendly interface, is portable, and can be programmed to perform a series of tests scheduled along days or months. An example of cement hydration process monitoring is presented to show the performances and versatility of the proposed system.

Profile Generator for Ultrasound Doppler Systems
Dario Russo, Valentino Meacci, Stefano Ricci

The rheological characterization of the fluids employed in food, pharmaceutical, chemical industries is of paramount importance for product quality and monitoring of the production process. Recently, embedded systems capable of non-invasive and in-line rheological fluid characterization are available. They are based on the Pulsed Ultrasound Velocimetry (PUV) technique, where the velocity profile of the fluid moving in a pipe is detected along the pipe diameter through Doppler ultrasound. The test and accuracy characterization of these systems is currently based on flow-rigs, which consist in hydraulic circuits where pumps push a test fluid along a pipe. Unfortunately, they are cumbersome, and the knowledge of the velocity profile developed in the pipe, to be used as ground-truth in accuracy tests, is limited. In this paper, a flexible testing system for PUV equipment is presented. It generates a radiofrequency signal that mimics the ultrasound Doppler signal produced in a flow-rig. The mimicked velocity profile is programmable and perfectly known. Tests with this generator connected to a PUV system are presented to show its flexibility.

Comprehensive Comparison of Null Convention Logic Threshold Gate Implementations
Kelby Haulmark, Wassim Khalil, William Bouillon, Jia Di

Asynchronous circuits offer many advantages including no clock, reliable operation, flexible timing requirement, and low electro-magnetic interference. NULL Convention Logic (NCL), as a popular quasi-delay-insensitive asynchronous design paradigm, incorporates threshold gates as its logic family. The implementations of these gates directly impact the performance of NCL circuits. This paper features eight NCL implementations published in literature and compares them across various metrics. The results and analysis can be used by designers for selecting the most appropriate design for their specific applications.

A2L-A: CAD and Electronic Design Automation
Session Type: Lecture
Location: Auditorium (Level 2)

On the Optimization of DT Incremental Sigma-Delta Modulators in Combination with CoI Reconstruction Filters
Johannes Wagner, Patrick Vogelmann, Maurits Ortmanns

In this paper the optimization of discrete-time incremental Sigma-Delta modulators in combination with chain-of-integrators reconstruction filters is described. In the state-of-the-art, the modulator and reconstruction filter part of an incremental Sigma-Delta ADC is usually designed separately, not necessarily leading to the best possible performance. By extending the automated design tool www.sigma-delta.de for the support of incremental Sigma-Delta ADCs, the modulator part can be optimized with regard to the reconstruction filter. It is shown that the performance of an incremental Sigma-Delta ADC can benefit from this combined optimization compared to an ADC consisting of a modulator optimized independently from the reconstruction filter. Moreover, the reproducibility of the optimization results can be improved.

Task Allocation and Scheduling Optimization in the Heterogeneous Core System
Ryota Tsuchihashi, Komei Nomura, Yasuhiro Takashima, Yuichi Nakamura

We propose a task allocation and scheduling (TAS) optimization for the varying execution time tasks in the heterogeneous core system. It utilizes the additional dependency called waiting dependency and optimizes the core type assignment by simulated annealing. We confirm that the proposed method improves the scheduling performance, empirically.

Automated Synthesis of Subsampling CT Bandpass Sigma-Delta Modulators with Non-Idealities
Johannes Wagner, Felix Vogel, Florian Kuhm, Maurits Ortmanns

In this paper the automated high-level synthesis of subsampling continuous-time bandpass Sigma-Delta modulators including non-idealities is described. State-of-the-art design methodologies for bandpass Sigma-Delta modulators involve multiple steps and transformations to derive high-level coefficients of CT modulators. Successive tuning to account for non-idealities is required in the design process which is even more time consuming. The web-based design-tool www.sigma-delta.de on the other hand allows the modulator synthesis within seconds, directly in the CT domain. Moreover, the STF is optimized with regard to a given specification while the SNR is maximized. This work shows the newly developed resonator models and the inclusion of subsampling capabilities in this design tool. The models are presented and circuit simulator based examples show the functionality.

Fast Approximate Algorithm for the Single Source Shortest Path with Lazy Update
Tomohiro Takahashi, Yasuhiro Takashima

In this paper, we propose a fast approximate algorithm of the Dijkstra algorithm which solves the single source shortest path problem (SSSP). In the conventional Dijkstra algorithm, one node with the minimum tentative distance is selected from unvisited nodes, and the tentative distances of its adjacent nodes are updated. In this method, its optimality is guaranteed by utilizing the fact that the tentative distance of the selected node will not be updated any more. However, there may be several nodes whose tentative distance will be updated. In this paper, we reduce the computation time by using the *Lazy Update* method which selects all of these nodes and determines their distances simultaneously. Moreover, if the error is allowed, it becomes much faster. By experiments, we confirm that it achieves about 10 times faster.

A2L-B: Nonlinear Systems and Applications

Session Type: Lecture

Location: Room 3 (Level 1)

Random Number Generator Based on Fuel Cells
Celal Erbay, Salih Ergun

Random number generators (RNG) are one of the most important building blocks of cryptosystems. Sensitive data are increasingly used in communication systems so generating unpredictable secret keys and random numbers play a significant role in cryptography for strong security and privacy measures. This paper presents RNG based on micro scale fuel cell array that is fabricated by using microfabrication techniques. A fuel cell converts the chemical energy into electricity by consuming the fuel such as hydrogen. Here, we use a microbial fuel cell to generate electricity and harvest the entropy during its operation then obtain strong random numbers from the generated electricity value after using hash function SHA-512 as post-processing. The NIST 800-22 statistical randomness test suite shows that fuel cells-based RNG can provide high-quality random numbers. This method provides secure data transfer directly without any other physical RNG where fuel cells needs to be used such as reactors, vehicles, portable electronic devices.

Hardware Implementation of Bio-Inspired Models
Zdenek Kolka, Viera Biolkova, Dalibor Biolek, Zdenek Biolek

The so-called hybrid approach to hardware emulation of bio-inspired devices and nonlinear dynamic processes of complex nature is proposed. Two issues are discussed: the stability of the emulation process and the possibility of partitioning the system into two parts, one being emulated digitally and the other via an analogue circuitry. The procedure is illustrated on the example of emulating the Fitzhugh-Nagumo model of neuron.

Analytical Modeling of Continuous-Time Chaos Based Random Number Generators
Kaya Demir, Salih Ergün

This paper presents an analytical study about regular sampling of a continuous-time chaotic signal to make random number generators (RNGs). The procedure of choosing the sampling frequency to produce random bits is explored using the concept of autocorrelation. To mathematically describe the distribution and statistical properties of the underlying chaotic state variable, Kernel density estimation and polynomial regression methods have been studied. Applying these two methods, probability density function of the chaotic signal was defined analytically. Using the probability density function, bit distribution probability of the RNG has been investigated.

Wearable System for Sensory Substitution for Prosthetics
Moustafa Saleh, Ali Ibrahim, Flavio Ansovini, Yasser Mohanna, Maurizio Valle

This paper presents a wearable system prototype based on commercial off-the-shelf components for sensory substitution for prosthetics. It provides a wireless portable interface electronics for tactile sensor array. The system transmits the acquired tactile information to the prosthetic user through electrotactile stimulation. An experimental setup has been carried out to validate the proposed prototype: results demonstrate the correct functionality when different input stimuli have been tested and conveyed to the stimulator. The proposed system overcomes similar state of art solutions dealing with higher number of input channels maintaining the real time functionality.

Diagonal Mode: a New Mode for Triboelectric Nanogenerators Energy Harvesters

Reem Abd El-Sttar, Endy Onsy, George Maximous, Ahmed Zaky, Tamer A. Ashour, Ashraf Seleym Seleym, Hassan Mostafa

In this work, a new diagonal motion mode is studied intensively in attached electrode regime and simulated using COMSOL MULTIPHYSICS. A complete analytical model of the proposed TENG model has been derived. In addition, a comparison between the analytical model and the COMSOL simulation results has been done. The maximum error between the results is equal to 5.3 % and the minimum error is equal to 0.88 %. The accuracy of the analytical model was a motivation for constructing a Verilog-A model to study the device under different loading conditions. A case of simple resistive load is considered, the results show that the open circuit voltage is equal to 5 V while the short circuit charge equals to 45 pC. The short circuit current is equal to 193 pA at theta of 0. Also, the peak power is equal to 50 pW for a load resistance of 110 GΩ.

A3L-A: Circuits and Systems for Communications

Session Type: Lecture
Location: Auditorium (Level 2)

Texture Super-Resolution in Multiview RGB-D Transmission

Julia Farrugia, Carl James Debono

Auto-stereoscopic displays allow viewers to experience 3D content by displaying multiple camera views. To reduce bandwidth requirements the multiview video plus depth (MVD) representation can be used, where only a subset of these camera views needs to be transmitted together with the depth maps. The display can then apply depth-image-based rendering techniques to reconstruct the missing views. In this work we propose further reduction in bandwidth through down-sampling of the texture views before encoding and then apply a dictionary-based super-resolution method during the up-sampling process at the receiver. The depth videos are still transmitted at full resolution. Multiview high efficiency video coding (MV-HEVC) is used to separately encode the texture and depth videos because of their different resolutions. The visual quality of the decoded and reconstructed content was evaluated through objective and subjective testing giving fair to good and poor to fair quality results for texture down-sampling by two and four respectively.

A Software Defined Radio Transceiver Based on Dynamic Partial Reconfiguration

Sherif Hosny, Eslam Elnader, Mostafa Gamal, Abdelrhman Hussien, Ahmed Hussein, Hassan Mostafa

Dynamic Partial Reconfiguration (DPR) has been used extensively over the past few years allowing reconfiguration of Field Programmable Gate Array (FPGA) during run time. With the aid of DPR, multi-standard Software Defined Radio (SDR) system can be implemented in order to save power and area extensively. In this paper, SDR is implemented using five wireless communication systems: Bluetooth, Wi-Fi, 2G, 3G, and LTE on the same reconfigurable hardware. A test environment is established to measure the effectiveness of the new technique using

Zynq-7000. A comparison is performed for the system total area and power consumption with and without DPR. This work achieves reduction of area and power by 10.19 % and 76.71 % respectively using DPR with an average switching time of 3.49 ms.

A Mixer-1st Auxiliary Receiver for Full-Duplex Self-Interference Cancellation
Dario Prevedelli, Giacomo Pini, Danilo Manstretta, Rinaldo Castello

This paper presents a low-power highly linear mixer-1st receiver to be used as an auxiliary receiver in a full- duplex transceiver architecture with self-interference cancellation. The auxiliary mixer-1 st receiver in-band performance, which is the most critical one for this application, is mainly determined by the baseband trans-impedance amplifier. The design is based on a wideband three-stage operational trans- conductance amplifier that draws 3 mA from a 1.8 V supply. A simple technique is presented to improve the achievable signal-to- noise-and-distortion ratio in this type of receiver designs. A prototype receiver implemented in a 28nm CMOS technology achieves a noise figure of 10 dB, in-band/out-of-band IIP3 of 11 dBm and 22 dBm respectively. The chip occupies an area of 640x490 μm^2.

A 20-60GHz Digitally Controlled Composite Oscillator for 5G
Yury Antonov, Markus Tormanen, Jussi Ryynanen, Aarno Parssinen, Kari Stadius

This paper describes a frequency generator supporting over-an-octave tuning range for 5G receiver front-end. Generator is built by composition of smaller-range oscillators multiplexed to the common output that drives a downconversion mixer. Simulated in 28nm CMOS with full physical device models the composite oscillator exhibits a frequency tuning range from 21.5 to 60.7 GHz (95.4%) dissipating 25.8 mW from a 0.9 V supply. As a result, it achieves -184dBc/Hz FOMTR.

Implementation of a C-V2X Receiver on an Over-the-Air Software-Defined-Radio Platform with OpenCL
Ming-Hsuan Lai, Tzi-Dar Chiueh

In this paper, we present a ready for real-time cellular vehicle-to-everything (C-V2X) receiver on a software-defined-radio (SDR) platform with Open Computing Language (OpenCL) demonstrated via an over-the-air (OTA) test platform. To meet the ultra-reliable and low latency communication (URLLC) requirement of V2X, we proposed and implemented several GPU programming techniques that significantly speed up the physical layer processing of the C-V2X receiver. With the specification of the new radio (NR) in fifth generation (5G) being just around the corner, the proposed OTA receiver can serve as a foundation for the quick development of NR C-V2X prototype with minor modification.

Modeling of a Re-Configurable Indoor Positioning System Based on Software Defined Radio Architecture
Giovanni Piccinni, Gianfranco Avitabile, Giuseppe Coviello, Claudio Talarico

This paper introduces the model of a software configurable indoor positioning system where the hardware of the active nodes is based on the Software-Defined Radio architecture. The use of an SDR architecture allows to vary the properties of the transmitted signal as function of the precision and the accuracy required by diverse applications and operating conditions. The target positions are extracted using a fully-digital algorithm implemented with an FPGA that can be easily extended or modified to improve the overall performance of the system.

A3L-B: VLSI Systems and Applications

Session Type: Lecture

Location: Room 3 (Level 1)

Constructing Effective UVM testbench for DRAM Memory Controllers

Khaled Salah

In this paper, a generic UVM-based verification architecture for DRAM memory controllers is proposed. The proposed architecture exploits the common features between different DRAM memory controllers to come up with common scenarios/tests. The proposed architecture is as configurable as possible. It uses minimum number of classes and methods. Moreover, it provides generic scoreboard and components. Besides, it provides a generic payload and high reusability for the stimulus and sequences.

2^n RRR: Improved Stochastic Number Duplicator Based on Bit Re-Arrangement

Ryota Ishikawa, Masashi Tawada, Masao Yanagisawa, Nozomu Togawa

In the fields of machine learning and image processing, cost-less circuits with low energy are required instead of extreme precision, and stochastic computing (SC), a type of approximate computing, is attracting attention. In SC, stochastic numbers (SNs), bit streams with values of the appearance rates of 1's, are used. SC enables calculations with simple circuits. To make the calculation results correct, duplication of an SN (generating an SN with the same value) is required when using the SN with the same value. The conventional SN duplicator composed of a flip-flop (FF) has a problem that the output SN only depends on the input SN. Therefore, if the FF-based duplicator is used in a circuit with re-convergence paths, the output SN becomes erroneous. This paper proposes an SN duplicator, 2^n RRR that can output more independent output by its improved flexibility of bit re-arrangement. With this duplicator, the errors of the hyperbolic tangent function are reduced by up to 50% compared to the

duplicator that we proposed previously. Also, up to more than 99.9% of the circuit area is reduced compared to the implementation of binary computing.

Design and Performance of Virtually Nonvolatile Retention Flip-Flop Using Dual-Mode Inverters
Daiki Kitagata, Shuu'Ichirou Yamamoto, Satoshi Sugahara

We propose a virtually nonvolatile retention flip-flop (VNR-FF) applicable to energy-efficient power-gating systems, which is suitable for SoCs used in smart mobile devices. The proposed VNR-FF can retain its data using ultralow shutdown-state voltage induced by power-switches in logic domains. The VNR-FF is configured with dual-mode inverters that act as a Schmitt trigger inverter during ultralow-voltage retention mode and as a conventional inverter during ordinary-voltage normal operation mode. Design methodologies of VNR-FFs are developed from the viewpoints of their leakage and speed performances. Energy, speed, and retention performances of VNR-FFs are computationally analysed.

Approximate-Computing Architectures for Motion Estimation in HEVC
Alberto Paltrinieri, Riccardo Peloso, Guido Masera, Muhammad Shafique, Maurizio Martina

Various types of approximate adders are implemented and synthesized in a previously developed hardware accelerator for the computation of motion estimation through the sum of absolute differences. The model is firstly validated in MATLAB and C++ and then after synthesis the error vs power is calculated in three possible versions, depending on where the adders are placed in the circuit.

Robust Functional Verification Framework Based in UVM Applied to an AES Encryption Module

Frank Plasencia Balabarca, Edward Mitacc Meza, Mario Raffo Jara, Carlos Silva Cárdenas

Over the time, the digital design industry has performed an outstanding role in the development of electronics. Hence, a great variety of designs are developed daily, these designs must be submitted to high standards of verification in order to ensure the 100% of reliability and the achievement of all design requirements. The Universal Verification Methodology (UVM) is the current standard at the industry for the verification process due to its reusability, scalability, time-efficiency and feasibility of handling high-level designs. This research proposes a functional verification framework using UVM for an AES encryption module based on a very detailed and robust verification plan. This document describes the complete verification process as done in the industry for a popular module used in information-security applications in the field of cryptography, defining the basis for future projects. The overall results show the achievement of the high verification standards required in industry applications and highlight the advantages of UVM against SystemVerilog-based functional verification and direct verification methodologies previously developed for the AES module.

A1P-C: Poster Session 1

Session Type: Poster

Location: Poster Area

Torque-Oriented Stepper Motor Control in FPGA

Valentino Meacci, Riccardo Matera, Dario Russo, Stefano Ricci

Stepper motors are widely employed in several daily applications, since their use is quite simple. Typically, a microcontroller (or a similar digital device) generates pulse-bursts and a direction bit to control a commercial power driver that produces the 2-phase currents feeding the motor windings. Despite its simplicity, this open-loop solution is sensitive to load variation and fails severely if the torque load exceeds the motor capacity. Closed-loop solutions based on Field-Oriented Control (FOC) solves the problem. However, they require heavy calculations and a dedicated hardware to control the motor currents. In this paper, a closed-loop solution is presented that avoids heavy calculations and demands the motor currents generation to the same commercial driver typically used for open-loop solutions. A low-cost Field Programmable Gate Array (FPGA) implements the algorithm and connects to the commercial power driver through the standard 2-signal interface (pulse-burst / direction bit). Experiments with a 1.1 Nm, two phases, 200-step/revolution hybrid stepper motor show the performance of the proposed method in a constant torque condition and during a position step movement.

A New FPGA-Based Controller Card for the Optimisation of the Front-End Readout Electronics of Charged-Particle Veto Detector at ALICE

Clive Seguna, Edward Gatt, Giacinto Decataldo, Ivan Grech, Owen Casha

The current Charged Particle Veto-detector (CPV) readout system of the ALICE (A Large Ion Collider Experiment) will be upgraded in 2018 for collecting more than 10 nb-1 of Pb- Pb collisions at luminosities of 6x1027cm^{-2}s^{-1}. The corresponding bandwidth of the detector must be increased by at least a factor of 10 from

4 kHz to a collision rate of 50 kHz for Pb-Pb particle collisions. The design of such a system is a challenging task, therefore various technologies and architecture topologies are being considered and investigated for the optimization of the front-end readout electronics. The upgrade proposed in this work has been tested and verified and preliminary results demonstrate that this work will enable CPV detector to reach interaction rate of at least 50 kHz or more. Optimization strategies include the use of a high-pin count 28 nm low-power FPGA technology for the simultaneous readout of digital signal processors called DiLogic cards, and use of high speed transceiver links at 3.125 Gbps.

Low Area and Low Power Implementation for Caesar Authenticated Ciphers
Amr Abbas, Ahmed Mohieldin, Hassan Mostafa

Authenticated Encryption (AE) and Authenticated Encryption with Associated Data (AEAD) play a significant role in cryptography as they simultaneously provide confidentiality, integrity, and authenticity assurances on the data. The Competition for Authenticated Encryption, Security, Applicability, and Robustness (CAESAR) seeks optimal authenticated ciphers based on multiple criteria, including security, performance, area, and energy-efficiency. In this paper, low area and low power implementations of selected ciphers from the CAESAR candidates namely NORX, Tiaoxin, SILC, and COLM are provided. A reduction in area with an average of 43% and a reduction in dynamic power with an average of 54% are achieved compared to their corresponding high-speed architectures. Moreover, throughput (TP) in (Mbps) decreases by an average of 68% and throughput-to-area (TP/A) in (Mbps/Slices) decreases by an average of 48%.

A Fixed-Point Natural Logarithm Approximation Hardware Design Using Taylor Series
Miguel Weirich, Guilherme Paim, Leandro Rocha, Eduardo Costa, Sergio Bampi

The logarithm function is employed in several areas of knowledge because its curve approximates various physical and chemical

phenomena. In this work, we propose an operator which can approximate the logarithm function at the natural base. Such an operator is implemented using Taylor Series approximation with five terms. We also offer an algorithm responsible for allowing input values different from the ones that are included in the convergence region of the Taylor Series. Through co-simulations using both the Matlab and ModelSim simulators, it was possible to determine that the approximation error remains less than 0.6 % for the entire input range. The input range used in this paper is in integer format with a one-byte length, and the system output has 19 bits with 4.15 form.

Real-Time Lane Detection-Based Line Segment Detection
Ahmed Mahmoud, Loay Ehab, Mohamed Reda, Mostafa Abdelaleem, Hossam Abdelmunim, Mohamed S. Darwish, Hassan Mostafa

This paper introduces a robust algorithm for real-time lane detection using the lane markers in urban streets or highway roads. It is based on applying Region of Interest (ROI) on the input image of the road from a calibrated camera in the front of the car, generating the top view of the image using Inverse Perspective Mapping (IPM), applying the core algorithm Line Segment Detection (LSD) which is followed by post-processing steps. Applying curve fitting to the line segments to get the right and left lines or curves. Finally, to get the output stream inverse IPM is applied. The proposed algorithm can detect the road lanes discriminating dashed and solid road lanes, straight and curved road lanes overcoming the shadow effect challenge with real-time performance 70 frames per second.

Design of an STM32F4 Microcontroller Development Board for Switching Power Converters
William Agius, Kris Scicluna, Joseph Zammit, Clive Seguna, Jeremy Scerri

Modern power electronic circuits typically require an on-board microcontroller to carry out necessary sensor measurements and controlled semiconductor switching. Hence, in the prototyping stage it is convenient to have a microcontroller development board designed for noise immunity and best electromagnetic

compatibility possible. Typical development boards provided by manufacturers are not designed to such a specification due to cost considerations. This paper presents the design of an improved development board for the STM32F4 microcontroller for better performance in switching power converter circuits.

AppropinQuo: a Platform Emulator for Exploring the Approximate Memory Design Space
Giulia Stazi, Antonio Mastrandrea, Mauro Olivieri, Francesco Menichelli

In this work we present AppropinQuo, a flexible and configurable emulator for embedded platforms with approximate memory. The emulator includes models of the effects of approximate memory circuits and architectures that depend on the internal structure and organization of the cells. The ability to emulate a complete platform, including CPU, peripherals and hardware-software interactions, is particularly important since it allows to execute the application as on the real board, reproducing the effects of errors on output. In fact, output quality is related not only to error rate but it also depends on the application, implementation and its data representation.

Power Optimization of a 0.5V 0.286-to-18MHz ADPLL in 65nm CMOS Process
Fredrick Angelo Galapon, Mark Allen Agaton, Arcel Leynes, Lemuel Neil Noveno, Anastacia Alvarez, Chris Vincent Densin

A clock generator is an important part of most systems as it is used for synchronization and data processing. For low-power operations, an all-digital phase-locked loop (ADPLL) is a suitable implementation of a clock generator for wireless sensing applications. Design decisions in different levels of abstraction were done to further reduce the power of an implemented ADPLL. It was shown that its power consumption can be minimized by at most 70 %. Moreover, the output frequency of the ADPLL ranges from 0.286-18 MHz with a power consumption of 4.606 μW at 18 MHz.

Characterization of Digital IC for Sub-Nanosecond Dead-Time Adjustment Used in Synchronous DC-DC Converters
Josip Bacmaga, Raul Blecic, Roger Voaden, Adrijan Baric

A digital integrated circuit for sub-nanosecond dead-time adjustment is characterized by time-domain measurements. The dead-time adjustment circuit (DTAC) generates two complementary control signals for the switches used in synchronous switching DC-DC converter application. The control signals are generated from a PWM signal that is applied from a signal generator to the input of the DTAC. The circuit is based on a tapped delay-chain architecture and it is designed for the switching frequencies up to 10 MHz. The DTAC is designed and fabricated in a 0.18-μm CMOS process. The characterization setup is shown and operating principle of the designed circuit is described. The generated dead times are measured for the whole range of the achievable discrete time-delay values at different switching frequencies.

Projected-Gradient-Descent in Rakeness-Based Compressed Sensing with Disturbance Rejection
Mauro Mangia, Letizia Magenta, Alex Marchioni, Fabio Pareschi, Riccardo Rovatti, Gianluca Setti

Compressed Sensing (CS) has recently emerged as an effective tool to simultaneously acquire and compress analogue waveforms in low-resource sensing devices. Its mechanisms have been also extended by both adapting the sensing stage to the actual class of input signals, and granting it the ability to reject disturbances. Regrettably, the resulting design flow entails the solution of two optimization problems with a potentially huge number of variables. This work overcomes this impasse by proposing a Project-Gradient-Descend method algorithm that drastically reduces the required CPU time to obtain a solution.

A2P-C: Poster Session 2

Session Type: Poster
Location: Poster Area

Characterization and Equivalent Circuit Model of 500-MHz Two-Port Electromagnetic Resonant Couplers for Isolated Gate Drivers

Raul Blecic, Josip Bacmaga, Adrijan Baric

Four two-port electromagnetic resonant couplers for isolated gate drivers are designed with the resonant frequency of 500 MHz. Each coupler is based on a different architecture and each occupies a different area. An equivalent circuit model is proposed and it is fitted to the Y- and Z-parameters, which are calculated from the S-parameters obtained by electromagnetic simulations. The couplers are processed on a printed circuit board and characterized by a vector network analyzer. The couplers are compared in terms of the transmission at the resonant frequency, 3-dB bandwidth and area they occupy.

Sensorless Position Tracking in Steer-by-Wire Using the Sonic Method

Kris Scicluna, Cyril Spiteri Staines, Reiko Raute

This paper presents the application of the Search-based Online Commissionable (SONIC) sensor-less observer algorithm to steer-by-wire in automotive applications. The tracking performance of the observer for both mechanical and electrical rotor positions for a Surface Mounted Permanent Magnet Synchronous Machine is shown. Typical steering transients and torque feedback were used which were determined experimentally from a street legal vehicle as part of this same research.

Development of a New Low-Cost EMG Monitoring System for the Classification of Finger Movement
Clive Seguna, Kris Scicluna, Jeremy Scerri

Electromyography (EMG) signals are commonly used by researchers to study kinesiology, which can then be used to control prosthetic arms, hands and limbs [1]. Additionally, EMG signals are used in the field of Bio Robotics for gesture control applications. The aim of this work is to implement a set of affordable active electrodes for the classification of finger movement via time-domain analysis. The electromyography signals are received through the Ag-AgCl electrodes, which are conductive materials used for gathering and transferring the muscle activation potential. The proposed paper focuses on presenting a new low-cost based system for the classification of human finger movement using auto-gain adjustment active electrodes. Different people will have different EMG amplitudes; therefore, it is difficult to determine the gain required prior performing further signal processing.

A Compact Low-Power Mitchell-Based Error Tolerant Multiplier
Aly Sultan, Ali H. Hassan, Khaled N. Salama, Hassan Mostafa

Power consumption is a crucial design aspect in multimedia and machine learning applications. Approximate computing offers an energy-efficient approach for both power reduction and area optimization. In this paper, a hybrid approximation methodology based on error tolerant multipliers (ETMs) is introduced. The proposed design splits the approximation process into two parts: (1) approximating the most significant bits (MSBs) using approximate logarithms and (2) approximating the least significant bits (LSBs) using truncation. A prototype of the proposed multiplier is demonstrated with an image processing application (JPEG compression) using a Discrete Cosine Transform (DCT) where the power delay product (PDP) is improved by 1.9X. And the area utilization is reduced by 2.7X with only 20 % reduction in the output image peak signal-to-noise ratio (PSNR).

Power System Frequency Estimation Using the Kernel Least Mean Square Algorithm and the Clarke Transform
Maicon Ferreira, Sergio Almeida, Eduardo Da Costa

In this work, we propose a methodology for frequency estimation of three-phase power systems using adaptive filtering based on the Kernel Least Mean Square algorithm (KLMS) in the complex form. Generally, abnormal data obtained from measurements may cause noises and affect the accuracy of frequency estimation in a power system. Thus, the proposed method is employed to suppress the abnormal data of measurements allowing greater efficiency in frequency estimation. Results of frequency estimation for distorted signals using the proposed method are compared with LMS algorithms presented in the current literature.

Hierarchical Floorplanning Based on Analog Structure Tree
Chao Geng, Shigetoshi Nakatake

In a hierarchical optimization framework for analogue designs, we introduce an analogue structure tree to floor planning which consists of device-, circuit-, structure-, and function-level groups. The structure tree is constructed such that each node corresponds to a proximity or a symmetry constraint is consistent with the layout. Furthermore, we modularize nodes at a specified level of the analogue structure tree and deal with them as soft modules in floor planning. In experiments, we demonstrate our system generates a reasonable layout of typical analogue circuits at a surprising speed compared with manual design.

Analog Retargeting Constraint Extraction Based on Fundamental Circuits and Layout Regularity
Xuncheng Zou, Shigetoshi Nakatake

This paper proposes a layout constraint extraction for CMOS analogue layout re-targeting. In this approach, first, we extract fundamental circuits such as current-mirrors and differential-pairs from a given net-list. Second, regular structures such as arrays and rows are extracted from a given layout which was

designed before. Finally, we generate layout constraint by matching the fundamental circuits and the regular structures. A retargeting case study is shown to apply our approach to a comparator design.

A Transient Noise Analysis of Secured Dual-Rail Based Logic Style
Kashif Nawaz, Itamar Levi, François-Xavier Standaert, Denis Flandre

Dual-rail logic circuits have been used as an effective countermeasure towards a more secure circuit design. However, with technology scaling and lowering of VDD, they lose interest as the signal reduction is less significant compared to CMOS. In this work, we revisit dual-rail logic designs (more specifically DDSLL) while focusing on intrinsic physical device noise using a transient noise analysis methodology and show that there exists a potential for such circuits to reduce the signal and concretely increase the noise. Our analysis, which extends to meaningful cryptographic figures-of-merit (FoMs) such as the SNR and Mutual-Information (MI), better clarifies the potential of DDSLL circuits to leverage the noise.

High-Resolution ADCs for Biomedical Imaging Systems
Hua Fan, Xinjie Wu

With the rapid development of biomedical imaging systems, the requirement of the accuracy of an Analog-to-Digital Converter (ADC) becomes more and more critical. Traditional Nyquist-rate analogue to digital data converters cannot meet the requirement any more. Sigma-Delta analogue to digital data converter, which makes a trade-off between speed and accuracy, can achieve an ideal accuracy by employing the oversampling and noise-shaping technology. In this work, a Verilog-AMS model for sigma-delta modulator is built, including the topologic, the order of stage, oversampling rate, system parameters, etc. On the basic of theoretical analysis and scientific flow path, finally, a third-order 1-bit sigma-delta modulator is designed and optimized, whose performance agrees well with the theoretical module.

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