1. The synchronous machine in Figure 1, having two inputs \( X_1 \) and \( X_2 \), and one output \( Z \) is to be implemented using a VHDL code. [PS – Present State].

(a) Write down a behavioural description of the above system using sequential VHDL code assuming that state transitions can only occur on the negative edge of a clock signal CK.

(b) The above system has to be tested using a testbench which supplies the signals shown in Figure 2:

![Figure 1](image1)

![Figure 2](image2)
Write down the VHDL code for the above testbench assuming that the clock period is equal to 8 ns.

(c) The testbench in (b) is to be connected to the system in (a). Write down the corresponding VHDL code together with a configuration file.

(d) Write down the VHDL code in order to implement a 4-bit up/down counter with carry.

2. The following diagram shows a linear sequential circuit used for data coding.

(a) Declare the D-Flip Flop entity together with its behavioural description using sequential VHDL statements. Assume that the setup and hold times are both 5 ns and that the reset signal is asynchronous.

(b) Write down the entity declaration and structural architecture of the whole coder using VHDL format. Assume that the XOR gates are stored in library WORK, with entity name XorGate and architecture name Basic. Hence write down the configuration file for the coder.

(c) Write down a behavioural description of the D-latch using VHDL language, assuming zero setup time and hold time.

(d) Briefly describe how a VHDL behavioural description can be written down starting from the state diagram of a sequential synchronous circuit.

(e) VHDL allows multiple configurations of the same entity. Explain why such a feature can be useful during the design cycle of a digital integrated circuit.
3. The following diagram shows a 4-bit first order digital integrator which can be used a variable frequency divider in a Direct Digital Synthesizer by taking the output from the carry out of the 4-bit adder. The frequency division ratio can be controlled by the 4-bit input word P.

![Diagram](image)

**Figure 4**

(a) Write down a behavioural description of the above system using a VHDL code. The system should have an asynchronous reset signal.

(b) Given that the input frequency is 20 MHz, write down the VHDL code for a testbench such that the above system gives an output frequency of 5 MHz.

(c) The testbench in (b) is to be connected to the system in (a). Write down the corresponding VHDL code.

4. A BCD adder adds two BCD numbers (each of range 0 to 9) and produces the sum in BCD form. For example, if it adds 9 (1001) and 8 (1000) the result would be 17 (1 0111). Implement such a BCD adder using a 4-bit adder and appropriate control circuitry in a VHDL code. Assume that the two BCD numbers are already loaded into two 4-bit registers (A and B) and there is a 5-bit sum register (S) available.

5. Using VHDL design a circuit that finds the closest integer square root of an 8-bit unsigned binary number N using the method of subtracting out odd integers. To find the square root of N, we subtract 1, then 3, then 5 and so on, until we can no longer subtract without the result going negative. The number of times we subtract is equal to the square root of N.

For example the square root of 27

\[
\begin{align*}
27 - 1 &= 26 \\
26 - 3 &= 23 \\
23 - 5 &= 18 \\
18 - 7 &= 11 \\
11 - 9 &= 2 \\
2 - 11 &= \text{negative. We subtracted 5 times and the root is therefore 5.}
\end{align*}
\]