Frequency Synthesizers

CCE 5220
RF and Microwave System Design
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Frequency Synthesis

- Phase Locked Loops:
  - Integer-N PLLs
  - Fractional-N PLLs

- DLL-based Frequency Synthesis:
  - Edge Combining Type
  - Re-circulating Type

- Direct Digital Synthesis:
  - ROM-based
  - Phase Interpolating
The Oscillator

- Fundamental building block in frequency synthesis.

- An electronic oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave or a square wave.

- **Harmonic (linear) oscillator**: produces a sinusoidal output. There are a few types of harmonic oscillators. The basic form of a harmonic oscillator is an electronic amplifier with an electronic filter connected in the feedback loop.

- **Relaxation oscillator**: produces a non-sinusoidal output, such as a square, saw-tooth or triangle wave. It contains an energy-storing element (a capacitor or, more rarely, an inductor) and a trigger circuit (a latch, Schmitt trigger, negative resistor, etc.) that periodically charges/discharges the energy stored in the storage element thus causing abrupt changes in the output waveform.
LC Tank Oscillators

L – Inductance
C – Capacitance
R – Loss

Transconductance Amplifier
$g_m$

$g_m \geq \frac{1}{R}$

Sustained oscillations

$$\frac{V_{out}}{I_{in}} = \frac{sL}{LCs^2 + s\frac{L}{R} + 1}$$

active device cancels the effect of the tank loss to provide sustained oscillations
LC Tank Oscillators

\[
\frac{V_{out}}{I_{in}} = \frac{sL}{LCs^2 + s\frac{L}{R} + 1}
\]

Underdamped Response

Sustained oscillations
LC Tank Oscillators

For monolithic integration, there are two principal topologies how oscillators can be designed: ring oscillators (relaxation) and LC tuned oscillators (harmonic), although wave-based oscillators are emerging as possible alternative, especially for high frequency of operation.

Usually LC-oscillators are more commonly employed, since they have good phase noise performance, because of their inherent band-pass filtering action that can suppress side-band noise, and outperform the other solution in terms of power consumption.

LC oscillators are also stable and robust towards temperature and process variations.

The price usually paid is less tuning-range since integrated variable capacitors have limited capacitance change with voltage.

In addition, a fundamental trade-off in such oscillators is tunability versus phase noise response.
Phase Noise and Jitter

- Phase noise and jitter are two measures of the same phenomenon: random fluctuations of the periodic time of an oscillator.

- Phase noise is associated with the frequency spectral representation whilst jitter is associated with the time domain representation of these fluctuations.
Phase Noise and Jitter

- An ideal sinusoidal oscillator can be mathematically described as:

  \[ V_{\text{out}}(t) = A \cos(2\pi f_0 t + \phi) \]

- with \( A \) being the amplitude, \( f_0 \) the frequency and \( \phi \) a fixed phase. In the frequency domain the spectrum of this oscillator consists of a Dirac-Impulse at \( f_0 \). The real oscillator is more generally modelled by:

  \[ V_{\text{out}}(t) = A(t) y(2\pi f_0 t + \varphi(t)) \]

- where \( y \) is a non-linear periodic function. The fluctuations introduced by the amplitude and phase result in sidebands close to the frequency of oscillation.
Phase Noise and Jitter

The frequency fluctuations correspond to jitter in the time-domain that is a random perturbation of the zero crossing of a periodic signal. Frequency fluctuations are usually characterized by the single sideband noise spectral density, $L_{SSB}$, normalised to the carrier signal power. It is defined as

$$L_{SSB}(f_0, \Delta f) = 10 \log_{10} \left( \frac{P_{\text{sideband}}(f_0 + \Delta f, 1\text{Hz})}{P_{\text{carrier}}} \right)$$

It has units of decibels below the carrier per Hertz (dBc/Hz). Note that $P_{\text{carrier}}$ is the carrier signal power at the carrier frequency $f_0$ and $P_{\text{sideband}}$ denotes the single sideband power at an offset from the carrier, both measured with a bandwidth of 1 Hz.
Phase Noise and Jitter

Examples:

GPS:
-105 dBc/Hz @ 1 MHz

Bluetooth:
-119 dBc/Hz @ 1.5 MHz
Phase Noise and Mixing

Channel

Adjacent Channel

Local Oscillator

Intermediate Frequency or Base Band
Phase Noise and Mixing

Channel

Adjacent Channel

Local Oscillator

Intermediate Frequency or Base Band
Example: GSM

- Channel Bandwidth (BW): 200 KHz
- SNR = 9 dB
- \[ L_{0.6 \text{ MHz}} = P_n - P_{\text{LO}} - 10\log_{10}(BW) \]
- \[ P_n - P_{\text{LO}} = P_{\text{channel}} - P_{\text{Interfere}} - \text{SNR} \]
- \[ P_n - P_{\text{LO}} = -99 + 43 - 9 = -65 \text{ dBm} \]
- \[ L_{0.6 \text{ MHz}} = -118 \text{ dBc/Hz} \]
- \( P_{\text{LO}} \): Oscillator Power
- \( P_n \): Noise Power
Time Domain Characterisation

- Consider an ideal oscillator (without noise) of periodic time $T_o$.

- In the presence of noise it will have an average periodic time $T_o$.

- The difference $T-T_o$ is the periodic jitter ($\sigma_T$ is the standard deviation)

$$E\{T\} = T_o$$

$$E\{(T - T_o)^2\} = \sigma_T^2$$

$$L(\Delta f) \approx 10 \log_{10} \left[ \frac{f_o}{(\Delta f)^2} \left( \frac{\sigma_T}{T_o} \right)^2 \right]$$

- Absolute Jitter (Long Term)

$$E\left\{ \left( \sum_{i=1}^{n} [T_i - T_o] \right)^2 \right\} = \sigma_{abs}^2$$

Time Domain Frequency Domain Relationship (white noise)
**Analogy with Phase Modulation**

\[ \omega_0 = 10.05 \text{ Hz} \]

- **Oscillator Model**
  \[ y = A_0 \sin(\omega_0 t + \phi) \]

- **Noise Perturbation**
  \[ \phi = A_n \sin(\omega_n t) \]

\[ A_n = 0.01 \]

\[ \omega_n = 2 \text{ Hz} \]
Analogy with Phase Modulation

\[ y = A_o \sin \omega_o t \cos \phi + A_o \sin \phi \cos \omega_o t \]

assuming small angle approximations

\[ y = A_o \sin \omega_o t + A_o \phi \cos \omega_o t \]

\[ y = A_o \sin \omega_o t + \frac{A_o A_n}{2} (\sin[\omega_o - \omega_n]t + \sin[\omega_o + \omega_n]t) \]

\[ 10 \log_{10} \left( \frac{P_{\text{sideband}}}{P_{\omega_o}} \right) = 10 \log_{10} \left( \frac{\left[A_o A_n\right]^2}{8 \frac{A_o^2}{2}} \right) = 10 \log_{10} \left( \frac{A_n^2}{4} \right) = -46.02 \text{ dBC/Hz} \]

\( A_n^2/2 \) is the total noise power at an offset frequency +/-2 Hz

Independent of oscillator’s amplitude
Phase Locked Loops

- The oscillators used in RF transceivers are generally integrated in a synthesizer environment so as to achieve a precise definition of the output frequency. There are generally two main types of frequency synthesizer architectures: **feedback architectures** and **feed-forward architectures**.

- A commonly employed feedback frequency synthesizer architecture is the **phase locked loop (PLL)**.

- A PLL is in essence a feedback system that aligns the clock edges of a **voltage controlled oscillator** with the edges of a high stability input reference oscillator.
Phase Locked Loops

- A phase detector compares the phase of a reference clock with that of the VCO output after its frequency has been divided.

- This phase difference is then low-pass filtered and used to set the frequency of the VCO. If the reference clock’s phase is ahead of the VCO output phase, the VCO will be forced to increase its output frequency until its phase has caught up.

- The frequency division in the feedback path allows the VCO output frequency to be at a multiple of the reference frequency, i.e. $f_{out} = M \times f_{ref}$.
Phase Locked Loops

Apart from providing a means to control the free running VCO to synthesize frequencies which are multiples of the reference clock, the PLL has also the important function of shaping the phase noise response of the VCO.

There exist two main types of PLL-based frequency synthesizers: integer-N PLL architectures and fractional-N PLL architectures.

In integer-N PLL architectures since the feedback divisor can be varied in integer discrete steps, the output frequency changes by only integer multiples of $F_{\text{ref}}$. This means that the channel spacing ($\Delta f$) is equal to $F_{\text{ref}}$ such that the loop bandwidth must be limited when a fine frequency resolution is requested.

$$\Delta F = F_{\text{out}_2} - F_{\text{out}_1} = NF_{\text{ref}} - (N-1)F_{\text{ref}} = F_{\text{ref}}$$
Phase Locked Loops

- Having a low bandwidth limits the minimum settling time of the PLL and in addition the PLL output will have a larger VCO phase noise contribution in the PLL close-in phase noise spectrum.

- For the same output frequency, a PLL with a larger feedback divisor increases the phase noise due to the reference clock at the PLL output.

- An alternative solution are Fractional-N PLL architectures in which the output frequency can be varied by a fraction of $F_{\text{ref}}$, allowing the latter to be much greater than the channel spacing thus a faster switching response can be achieved.

- The major disadvantage of Fractional-N PLL is the generation of more spurious tones than in an Integer-N PLL, but techniques have been investigated to lower their energy in the PLL output frequency spectrum.
Analogue PLL – The Origin

Analogue Multiplier (Phase Detector)

Loop Filter

Voltage Controlled Oscillator

Phase Error Filtered Term

Quadrature Phase Detector

\[ A \sin \phi_{in} B \cos \phi_{out} = AB \frac{\sin(\phi_{in} - \phi_{out})}{2} + AB \frac{\sin(\phi_{in} + \phi_{out})}{2} \approx AB \frac{\phi_{in} - \phi_{out}}{2} + AB \frac{\sin(\phi_{in} + \phi_{out})}{2} \]
Analogue PLL - Simulations

Frequency Error

Normalised Phase Error

Phase Error

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Analogue PLL - Simulations

Initial Transient ($F_{out} = 1$ MHz $F_{in} = 2$ MHz)
Analogue PLL - Simulations

Locked State Transient (F_{out} = 2 MHz F_{in} = 2 MHz)
Phase/Frequency Detectors

Phase Detector

Capture Range: $-360^0 < \Phi < 360^0$
Loop Filters – Passive Type

Advantages:
- Linear
- Relatively low noise
- Unlimited frequency range

Disadvantages:
- Hard to integrate when the values are large \((C>100\text{pF} \text{ and } R > 100k\Omega)\)
- Difficult to get a pole at the origin (increase the order of the type of PLL)

\[
H_{LF}(s) = \frac{1}{s\tau_1 + 1} \quad \text{where} \quad \tau_1 = R_1C_1
\]

\[
H_{LF}(s) = \frac{s\tau_1 + 1}{s\tau_2 + 1}
\]

where \(\tau_1 = R_2C\) and \(\tau_1 = (R_1 + R_2)C\)
Loop Filters – Active Type

Advantages:
- Can get poles at the origin
- Can reduce the passive element sizes using transresistance

Disadvantages:
- Noise
- Power
- Frequency limitation

\[ H_{LF}(s) = -\frac{s\tau_2 + 1}{s\tau_1} \]

where \( \tau_1 = R_1C_2 \) and \( \tau_2 = R_2C_2 \)
Loop Filters – Active Type

Active lag filter-I

\[ F(s) = -\frac{R_2 + \frac{1}{sC_2}}{R_1 + \frac{1}{sC_1}} = -\left(\frac{C_1}{C_2}\right)\left(\frac{sR_2C_2 + 1}{sR_1C_1 + 1}\right) \]

\[ = -\left(\frac{C_1}{C_2}\right)\left(\frac{s \tau_2 + 1}{s \tau_1 + 1}\right) \]

\( \tau_1 = R_1C_1 \) and \( \tau_2 = R_2C_2 \)

Active lag filter – II

\[ F(s) = -\frac{1}{R_2sC_2} \frac{1}{R_1 + \frac{1}{sC_1}} = -\left(\frac{R_2}{R_1}\right)\left(\frac{sR_1C_1 + 1}{sR_2C_2 + 1}\right) = -\left(\frac{R_2}{R_1}\right)\left(\frac{s \tau_1 + 1}{s \tau_2 + 1}\right) \]
Charge Pump PLLs

- The use of the PFD permits the use of a charge pump in place of the conventional PD and low pass filter. The advantages of the PFD and charge pump include:
  - The capture range is only limited by the VCO output frequency range
  - The static phase error is zero if the mismatches and offsets are negligible.

System is effectively sampled @ $F_{\text{ref}}$ – note effect on Bandwidth (BW): $BW < F_{\text{ref}}/2$
Loop Filters for Charge Pump PLL

Second-Order PLL:

Third order PLL:
Voltage Controlled Oscillators

This is generally tuned to change oscillation frequency

\[ f_{osc} = \frac{1}{2\pi\sqrt{LC}} \]

Active device to enable sustained oscillations

MOS transistor used as a varactor
VCO – Phase Noise Characterisation

- Leeson’s heuristic expression for the phase noise of an LC tank VCO:

\[
L_{SSB}(\Delta \omega) = 10 \log_{10} \left[ \frac{FkT}{2P_{\text{carrier}}} \left( 1 + \left( \frac{f_o}{2Q_L f_m} \right)^2 \right) \left( 1 + \frac{\Delta f}{f_m} \right) \right]
\]

\[
L_{SSB}(\Delta \omega) \approx 10 \log_{10} \left[ \frac{FkT}{8Q_L^2 P_{\text{carrier}}} \left( \frac{f_o}{f_m} \right)^2 \right]
\]

- F – Noise Figure
- K – Boltzmann’s Constant
- T – Temperature (Kelvin)
- Q_L – Loaded Q-factor
- f_m – offset frequency
- f_o – oscillation frequency

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VCO – Tuning Range Figure of Merit

To compare the performance of different VCOs the Tuning Range Figure of Merit (FOM\(_T\)) is generally used:

\[
FOM_T = 20 \log_{10} \left( \frac{f_o FTR}{10 f_{offset}} \right) - L\left( f_{offset} \right) - 10 \log_{10} (P_{DC})
\]

where \( f_o \) is the oscillation frequency, \( FTR \) is the tuning range expressed as a percentage, \( f_{offset} \) is the offset frequency at which phase noise \( L(f_{offset}) \) is measured and \( P_{DC} \) is the power consumption in milliwatts.

The higher the value of the FOM\(_T\) the better the performance of the VCO will be. The FOM\(_T\) value is used to compare different oscillators in a fair way by normalising the phase noise, by the power consumption, oscillation frequency and tuning range.
Frequency Dividers

- Dividers constitute a main function in PLL circuits.
- Generally a PLL needs to cover a very wide range of continuous divisions.
- Low speed dividers (up to a few 100 MHz)
  - Programmable Counters
- High speed dividers
  - Dual Modulus P/P+1 Dividers
Dual Modulus P/P+1 Dividers

- Dual Modulus dividers are employed to achieve a simple continuous division mechanism.

- A “P/P+1” dual modulus divider will divide by either P or P+1 based upon external command. It has a Modulus Control (MC) input port controlling the number of times to divide by P or P+1.

\[ P^2 - P \] is the lowest continuous divide ratio
Dual Modulus 2/3 Divider

When MC = 1 this flip flop is always reset

MC = 1 ÷2
MC = 0 ÷3
Dual Modulus Divider

- A complete PLL “N” divider is typically implemented using a dual modulus divider controlled by 2 programmable counters.

Problem B >= A Requirement will make some N values unachievable.
Dual Modulus Divider

- Initially the P+1 prescalar is used.
- Every P+1 cycles of the VCO, both the A and B counters are decreased by 1.
- This is continues until A = 0. This takes a total of \(A(P+1)\) VCO cycles.
- Now prescalar P is switched in. Every P VCO cycles, the B counter is decreased by 1. Since the B counter was previously counting, this takes \((B-A)P\) VCO cycles to go to zero.
- When the B counter reaches 0, one pulse is given to the feedback signal.
- This results in a division ratio of:
  \[N = A(P-1) + (B-A)P = P*B + A\]
Example

- A divide value of \( N = 960 \) is accomplished by dividing the input signal by 16 a total of 60 consecutive times. Changing \( N \) to 961 requires that we divide the signal by 16 a total of 59 times and then divide the signal by 17 once, and so on.

- If we need to generate divisions in the 100-150 range using a 16/17 device there will be some numbers that cannot be generated. A divide ratio of 100 can be gained by dividing twice by 16 and 4 times by 17 (\( 17 \times 4 + 16 \times 2 = 100 \)). However, there is no combination of 16 and 17 that can generate the number 103.

- To generate contiguous division numbers in this range would require a lower dual modulus (8/9, 10/11, etc).

- To run high division numbers and allow lower divisions (lower than \( P^2-P \)), tri-modulus and even quad-modulus circuits are used.
Dual Modulus Divider

- $N = A^*(P+1) + (B-A)*P = P*B + A$
- $A = 0 \ldots P-1 \quad A = N \mod P$
- $B \geq A \quad B = N \div P$
- $N_{\min} = P*B_{\min} + A_{\min} = P*(P-1) + 0$
- $N_{\min} = P^2 - P$
Fundamental Control Theory

\[ e = r - y_m \]
\[ y_m = H(s) \times y \]
\[ y = G(s) \times e \]
\[ y_m = G(s)H(s) \times e = G(s)H(s) \times (r - y_m) \]
\[ y_m(1 + G(s)H(s)) = G(s)H(s) \times r \]
\[ H(s) \times y \times (1 + G(s)H(s)) = G(s)H(s) \times r \]
\[ \frac{y}{r} = \frac{G(s)}{1 + G(s)H(s)} \]
PLL Modelling (Continuous Time)

- A typical PLL is in essence a sampled data system (the phase comparison is done in a discrete time manner).

- One can usually use a continuous model when the sampling frequency controlled by the reference clock frequency is generally much higher than the loop bandwidth.

- This ensures the phase lag introduced by the sample and hold operation of the digital components such as the phase detector can be ignored.
Example: Integer-N PLL

- An integer-N PLL uses a frequency reference oscillator running at 25 MHz, and a divide-by-100 reference divider. The output frequency band is 100-800 MHz. The VCO has a tuning coefficient of 100 MHz/V and the phase detector gain is 1 V per radian error. An active loop filter shown on slide 27 is used. Determine:

  - the active loop filter component values given that the resonant frequency of oscillation of the loop has to be 100 kHz and the loop is to be critically damped when the output frequency is 450 MHz.

  - the worst case switching time required by the PLL to hop from one channel to an adjacent in order to guarantee an output frequency error of not more than 0.1 kHz.
Modelling in Matlab

```matlab
1 - clear all; clc; close all;
2 - numv = [3.18e-6 1];
3 - denv = [0.688e-6 1];
4 - Gf = tf(numv,denv); % Loop filter
5 - GPD = 1; % Phase Detector
6 - numv = 2*pi*100e6;
7 - denv = [1 0];
8 - GVCO = tf(numv,denv); % VCO
9 - div = 1800; % Divider
10 - G = GPD * Gf * GVCO; % Feedforward Transfer Function
11 - CLTF = G/(1+G/div); % Closed loop Transfer Function
12 - OLTF = G/div; % Open Loop Transfer Function
13 - figure(1);
14 - step(CLTF,80e-6);
15 - grid on;
16 - w = linspace(2*pi*10e3,2*pi*1500e3,1000);
17 - figure(2);
18 - bode(CLTF,w);
19 - grid on;
20 - figure(3);
21 - bode(CLTF,w);
22 - grid on;
23 - figure(4);
24 - pzmap(CLTF);
```

Closed Loop Transfer Function:

\[
\frac{y}{r} = \frac{G(s)}{1 + G(s)H(s)}
\]

Open Loop Transfer Function:

\[
\frac{y_m}{e} = G(s)H(s)
\]
Modelling in Matlab

>> GCO
Transfer function:
6.283e008
-----------
 s

>> Gf
Transfer function:
3.10e-006 s + 1
--------------
 6.04e-007 s

>> CLTF
Transfer function:
0.001765 s^3 + 555.4 s^2
---------------------------------------------
7.815e013 s^4 + 9.813e007 s^3 + 0.3085 s^2

>> OLTF
Transfer function:
1.11 s + 3.491e005
--------------------
 8.84e-007 s^2

Second order linear system:

\[ s^2 + 2\xi \omega_n s + \omega_n^2 \]

where \( \xi \) – damping ratio
\( \omega_n \) – resonant frequency

\[\begin{align*}
\omega_n &= \sqrt{0.3086/7.815\times10^{-13}} \\
\omega_n &= 6.2840\times10^5 \text{ rad/s} \\
f_n &= 100 \text{ kHz} \\
\xi &= 9.813\times10^{-7}/(\omega_n \times 2 \times 7.815\times10^{-13}) = 1
\end{align*}\]
Modelling in Matlab

100 kHz resonant frequency and critical damping ($\xi=1$)

- Pole: $-6.28\times10^5 \pm 2.61\times10^4 i$
  - Damping: 0.999
  - Overshoot (%): 0
  - Frequency (rad/sec): $6.28\times10^5$
- Pole: $-6.28\times10^5 - 2.61\times10^4 i$
  - Damping: 0.999
  - Overshoot (%): 0
  - Frequency (rad/sec): $6.28\times10^5$
- Zero: $-3.14\times10^5$
  - Damping: 1
  - Overshoot (%): 0
  - Frequency (rad/sec): $3.14\times10^5$
- Zero: 0
  - Damping: -1
  - Overshoot (%): 0
  - Frequency (rad/sec): 0

System: CLTF

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Modelling in Matlab (OLTF)

Bode Diagram

Phase Margin = 76°
Modelling in Matlab (CLTF)

Bode Diagram

Magnitude (dB)

Phase (deg)

Frequency (rad/sec)

20\log_{10}(N)
Modelling in Simulink

Diagram of a phase detector, loop filter, VCO, divider, and channel selection.
Modelling in Simulink

Changing from $N = 3200$ to $N = 3199$

$T_{sw} \sim 21 \mu s$

Changing from $N = 3199$ to $N = 3200$

$T_{sw} = -\frac{\ln\left(\frac{df}{dF}\right)}{\xi\omega_n}$
Phase Noise Shaping

- Apart from providing a means to control the free running VCO to synthesize frequencies which are multiples of the reference clock, the PLL has also the important function of shaping its phase noise response.

- Obviously since the PLL is composed of other components, their effect on the closed loop phase noise response needs to be assessed.

- The evaluation of the phase noise response of the whole PLL by transient simulation is impractical due to the substantial amount of time required, mainly due to the presence of the prescalar in the feedback path.

- Hence, the model shown below is used to evaluate the total phase noise response due to the various noise components in the PLL.
Phase Noise Shaping

clc;
close all;

[REFPNf,f]=psd(REFPN,length(REFPN),1/1e-8);

[PLLf,f]=psd(PLL,length(PLL),1/1e-8);

semilogx(f,10*log10(PLLf)-10*log10(REFPNf),'
linewidth',3);

xlabel ('Frequency (Hz)');
ylabel ('\phi_{\text{out}} / \phi_{\text{ref}}');
grid on;
The phase noise of the reference clock at an offset frequency less than the bandwidth (100 KHz), needs to be low since it will be amplified by the multiplication factor (N). The phase noise is given by the equation:

\[ \frac{\phi_{\text{out}}}{\phi_{\text{ref}}} = \frac{2\pi K_d K_{\text{vco}}}{\tau_1} (s \tau_2 + 1) \]

\[ \phi_{\text{ref}} = \frac{2\pi K_d K_{\text{vco}}}{\tau_1 N} (s^2 + \left(\frac{2\pi K_d K_{\text{vco}} \tau_2}{\tau_1 N}\right) + \frac{2\pi K_d K_{\text{vco}}}{\tau_1 N} \]

where \(\phi_{\text{out}}\) is the phase noise at the output, \(\phi_{\text{ref}}\) is the phase noise of the reference, \(K_d\) and \(K_{\text{vco}}\) are constants, and \(\tau_1\) and \(\tau_2\) are time constants.
Within the bandwidth of 100 kHz the PLL is able to lower the phase noise of the stand-alone VCO.
PLL Phase Noise Shaping

VCO noise (1/f² noise)

PLL noise due to VCO

~ 80 dB
Spurious Tones

- Apart from the phase noise response of a PLL another important property is its spurious signal level.

- Spurious outputs or spurs are generated due to a discrete deterministic noise/ripple signal in the PLL architecture.

- There are mainly two types of spurs:
  - direct injection spurs
  - mixing spurs

- Direct injection spurs can be either generated by a finite ripple on the oscillator control signal at the reference clock frequency (reference spurs), or by a finite ripple on the PLL supply (supply injected spurs) whose magnitude is determined by the finite PSRR of the PLL blocks.

- Mixing spurs can result because of nonlinear operations such as clock edge squaring and phase detector chopping action which are capable of creating intermodulation frequencies. If the intermodulation spurs fall in the PLL bandwidth where minimal rejection exists large output spurs can be generated requiring high PSRR regulators. Note also that spurs in the reference clock are amplified by the PLL gain and translated to the output.
Fractional-N PLL

- In integer-N PLL architectures since the feedback divisor can be varied in integer discrete steps, the output frequency changes by only integer multiples of $f_{\text{ref}}$.

- This means that the channel spacing is equal to $f_{\text{ref}}$ and so for fine channel selection the loop bandwidth must be limited since $f_{\text{ref}}$ would be small.

- Having a low bandwidth limits the minimum settling time of the PLL and in addition the PLL output will have a larger VCO phase noise contribution in the PLL close-in phase noise spectrum.

- Another issue is that for a given output frequency, the division ratio $N$ must be large in order to permit a small $f_{\text{ref}}$. Since the phase noise of the reference clock is increased by a factor of $20\log_{10}(N)$ this increases the phase noise at the output at low offset frequencies.
Fractional-N PLL

An alternative solution are Fractional-N PLL architectures in which the output frequency can be varied by a fraction of \( f_{\text{ref}} \), allowing the latter to be much greater than the channel spacing thus a faster switching response can be achieved.

It possible to alter the relationship between \( N, f_{\text{ref}} \), and the channel spacing of the synthesizer. It is now possible to achieve frequency resolution that is a fractional portion of \( f_{\text{ref}} \). This is accomplished by adding internal circuitry that enables the value of \( N \) to change dynamically during the locked state. If the value of the divider is “switched” between \( N \) and \( N+1 \) in the correct proportion, an average division ratio can be realized that is \( N \) plus some arbitrary fraction, \( K/F \). This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing.

\[ F_{\text{vco}} = f_{\text{ref}}(N + K / F) \]

Where: \( F \) = The fractional modulus of the circuit
\( K \) = The fractional channel of operation.

The major disadvantage of Fractional-N PLL is the generation of more spurious tones than in an Integer-N PLL but techniques have been investigated to lower their energy in the PLL output frequency spectrum.

\[ \text{Channel Spacing} = \frac{f_{\text{ref}}}{F} \]
Fractional-N PLL

When $C_{\text{out}}$ is high a 1 is added to the value of $A$

$N = 32M + A$

$N_{\text{div}} = \frac{K}{F} (N + 1) + \frac{F - K}{F} (N)$

$N_{\text{div}} = \frac{K}{F} + N$
Fractional-N PLL: Example

F: 4  K: 1

Acc: 0 1 2 3 0 1 2 3 0

C_{out}: 0 0 0 0 1 0 0 0 1

C_{out} is high for K/F = \frac{1}{4}

F_{ref} is divided by N+1 for \frac{1}{4} of the time. For the rest it is divided by N

\begin{align*}
N_{div} &= \frac{1}{4}(N + 1) + \frac{3}{4}(N) \\
N_{div} &= \frac{1}{4} + N
\end{align*}
Delay Locked Loop

- Another form of feedback frequency synthesizer architectures are delay locked loops (DLL).

- They are very similar to a PLL with the difference that they make use of a voltage controlled delay line instead of a VCO to synthesize the required output frequency.

- DLL-based frequency synthesizers have limited phase noise accumulation and can be designed as a first-order system to allow wider loop bandwidth and thus very small settling times.
Delay Locked Loop

(a) Edge combining DLL-based frequency multiplier (b) VCDL with edge combiner: each delay stage DN consists of two inverting variable delay cells (c) Concept of a multiply-by-4 DLL-based frequency synthesizer
Direct Digital Synthesis

\[ F_{out} = \frac{2^N}{2^N + P} F_{in} \]
Direct Digital Synthesis

Direct Digital Synthesis (DDS) is another approach to achieve the same goal with certain advantages and disadvantages with respect to feedback architectures. The basic concept in a DDS is to generate the signal in the digital domain and utilise digital to analogue conversion together with filtering to reconstruct the waveform in the analogue domain.

DDS offers a number of advantages over phase-locked or feedback architectures, namely:

- it achieves a low phase noise roughly equal to that of the reference clock and does not require the use of an analogue VCO
- it provides very fine frequency steps
- it exhibits much faster channel switching than PLLs since it does not include any feedback loop
- it allows direct modulation of the output signal in the digital domain

These advantages come at the cost of generation of spurious tones which must be compensated for and an increased effort to design low power fast digital to analogue converters.
References