CCE1010 – Computer Logic 1

LAB #1 – Characteristics of Logic Gate Families

Equipment / Materials:

Oscilloscope dual trace 20 MHz
Signal Generator
Power Supply 5 V

TTL gates:
74LS04 inverter, 74LS14 schmitt inverter, 74LS06 open collector inverter

CMOS gates:
4069 inverter, 4011 NAND, 4001 NOR

E1. Determination of device characteristics of TTL and CMOS logic families:

Determine the:
(a) Power dissipation (P_H, P_L);
(b) Propagation delay (T_{PLH}, T_{PHL}) and speed-power product;
(c) Input-Output Transfer characteristic;
(d) Input current (I_{IL}, I_{IH});
(e) Maximum output current;
for the following devices: 74LS04 TTL inverter, 4069 CMOS inverter, 74LS14 schmitt trigger inverter.

E2. Verification of logic operation:

(a) Select appropriate CMOS gates in order to verify the operation (truth table) of the following 2-input gates - NAND, NOR, NOT.

(b) Build AND, OR, XOR, BUFFER circuits using only CMOS NAND/NOR or INVERTER gates.

E3. CMOS -TTL and open-collector interfacing:

(a) Interface a CMOS inverter input to a TTL inverter output and verify its operation;
(b) Interface a TTL inverter input to a CMOS inverter output and verify its operation;
(c) Select a TTL open collector inverter and use to drive an L.E.D. Hence verify its operation;
(d) Connect 4 TTL open collector TTL inverters in wired-NOR configuration and verify their operation.
E4. Combinational Logic Design:

A power pack contains five main parts - two main batteries and three auxiliary batteries. The power pack is safe to deliver power when the two main batteries and any two of the auxiliary batteries are fully charged. The inputs to the circuit to be designed consist of 5 signals for each battery state (low – uncharged, high – fully charged).

Your circuit should have 5 inputs and 6 outputs. The outputs are indicator lights; the first five simply indicate the status of the batteries. Each of these should illuminate when the battery is fully charged. The sixth output is the warning light and it should go on when the power pack is no longer safe to operate.

Procedure:
1) Design your circuit on paper using only CMOS 4000 series NAND, NOR and inverter gates
2) Build the circuit on the breadboard
3) Test all the possible inputs and write down the truth table for all of the 32 possible input combinations.

Preparation work:

1) Devise the test setup to be used in order to extract the performance characteristics in E1. Also obtain the respective datasheets for the ICs to be used.
2) Determine the IC part numbers to be used in E2 and E3 and obtain datasheets for the pinouts.
3) Design the circuit in E4. Draw the complete circuit including the ICs to be used with the pin numbers indicated.