ASIC Interface Design for Resonating Micro-Mirror MOEMS Spectrometer

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ABSTRACT

In recent years there has been an increased interest in air quality monitoring both at large scale and small scale. One useful tool to identifying different gases in the air is an IR absorption spectrometer. This device measures the attenuation of various spectral lines as an IR beam passes through a sample of the air in order to measure the concentration of individual gases. With the miniaturisation of air quality sensors, the move from benchtop spectrometers to micro-spectrometers is becoming more popular.

A commonly-used approach for IR micro-spectrometers uses an IR detector array to determine the spectral response of an IR beam. However, increasing the spectral resolution of such a micro-spectrometer requires a proportional increase in the number of pixels in the detector, significantly increasing the fabrication costs of the detector. An alternative approach uses micro-mirrors in order to sweep a diffracted IR beam over a single IR sensor, where the spectral resolution does not depend on the number of pixels but on the accuracy of the micro-mirror angular position. For such an approach a precisely controlled micro-mirror with a known frequency and oscillation amplitude is needed. In this research an innovative closed loop controller for achieving such precision is presented. The controller has been developed by designing individual blocks which have been simulated and evaluated separately. The complete digital controller is then implemented on an FPGA for initial testing and then converted for implementation as an ASIC where the high voltage circuitry necessary to drive the electrostatically-actuated micro-mirror is also integrated, leading to a more compact implementation. The fabricated prototypes are then tested using an optical testbench.

An analysis of the different waveforms that can be used to drive the micro-mirror and the ideal phase between the applied waveform and the micro-mirror angle is first carried out and used as a basis for the design of an all-digital closed loop controller. An improvement over previously published micro-mirror oscillation amplitude and phase measurement technique is then presented. This technique can be implemented in an all-digital controller since it relies on timing measurements from pulses generated by a single photodiode in the path of a reflected laser beam. An analysis is also carried out on different approaches that can be used to change the duty cycle of the drive waveform in order to change the amplitude of oscillation of the micro-mirror.

The mentioned innovations are used to design an all-digital micro-mirror closed loop controller. The controller was simulated in MATLAB Simulink before implementation on an FPGA in order to verify its ability to control the micro-mirror. It is also demonstrated that the output signal of the controller can be synthesised using an adapted dithering-based fractional-N divider.

The proposed controller is also implemented together with a high voltage output driver on the XFAB XT-018 BCD-on-SOI in order to demonstrate its feasibility of implementation in commercial applications. It is shown that the proposed controller is effective in accurately controlling the micro-mirror oscillation amplitude and thus validating the design.

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List of Publications

The following is a list of peer-reviewed publications resulting from this research work:

- B. Portelli, R. Farrugia, I. Grech, O. Casha, J. Micallef and E. Gatt, "Capacitance measurement techniques in MOEMS angular vertical comb-drive actuators," 2017 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), Bordeaux, France, 2017
- B. Portelli, I. Grech, J. Micallef, R. Farrugia, O. Casha and E. Gatt, "Resonant micro-mirror oscillation amplitude measurement and all digital actuation," 2020 Symposium on Design, Test, Integration & Packaging of MEMS and MOEMS (DTIP), Lyon, France, 2020, pp. 1-4.
- B. Portelli, I. Grech, J. Micallef, R. Farrugia, O. Casha and E. Gatt, "Resonant micro-mirror electrical characterisation towards tunable digital drive circuit design," 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, UK, 2020, pp. 1-4.
- B. Portelli, I. Grech, J. Micallef, R. Farrugia, O. Casha and E. Gatt, "Implementation of an all-digital electrostatic micro-mirror controller," 2023 Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP), Valetta, Malta, 2023, pp. 1-4

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List of Abbreviations

ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
AVC	Angular Vertical Combs
BCD	Bipolar-CMOS-DMOS
BCD	Binary Coded Decimal
BW	Bandwidth
CMOS	Complementary Metal-Oxide Semiconductor
CO2	Carbon Dioxide
CTS	Clock Tree Synthesis
DAC	Digital to Analogue Converter
DAsPLL	Digital Asynchronous Phase Looked Loop
DC	Direct Current
DDS	Direct Digital Synthesizer
DMOS	Discrete Metal-Oxide Semiconductor
DRC	Design Rule Checker
DRV	Design Rule Violation
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
FEA	Finite Element Analysis
FEM	Finite Element Modelling
FFL	Frequency Locked Loop
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IoT	Internet of Things
IR	Infrared

LVS	Layout versus Schematic
MEMS	Micro-Electro-Mechanical Systems
MOEMS	Micro-Opto-Electro-Mechanical Systems
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPW	Multi-Project Wafer
NIR	Near Infrared
NMOS	N-channel Metal-Oxide Semiconductor
PCB	Printed Circuit Board
PLL	Phase locked loop
PMOS	P-channel Metal-Oxide Semiconductor
PSD	Position Sensitive Detector
PWM	Pulse Width Modulation
PZT	Lead Zirconate Titanate
RAM	Random Access Memory
ROM	Read Only Memory
RTL	Register-Transfer Level
RMSE	Root Mean Squared Error
SOI	Silicon on Isolator
SPI	Serial Peripheral Interface
SVC	Staggered Vertical Combs
TNS	Total Negative Slack
TTL	Transistor–Transistor Logic
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VCO	Voltage controlled oscillator
VGA	Variable Gain Amplifier
VHDL	VHSIC Hardware Description Language
VHSIC	Very High-Speed Integrated Circuit
VOC	Volatile Organic Compound
WNS	Worst Negative Slack

1 Introduction

Near Infrared (NIR) spectroscopy has been used in various fields for detecting different gases at a variety of concentrations. A common application is in the analysis of air quality monitoring where concentrations of gases such as volatile organic compounds (VOCs) and carbon dioxide (CO_2) are measured [1, 2 ,3]. Traditional NIR spectrometers are bulky and expensive devices which limit their widespread use. Recently, NIR micro-spectrometers have been introduced. These devices use MEMS and other micro-fabrication technologies to reduce their size and cost [4, 5, 6].

The compact size and portability of micro-spectrometers make them suitable for deployment in a variety of settings, from urban areas to remote locations and industrial facilities. Their small footprint allows for easy integration into air quality monitoring networks, on vehicles, drones, or other internet of things (IoT) networked devices. This versatility enables the collection of data in real-world scenarios, providing valuable insights into air quality dynamics and trends.

The first NIR micro-spectrometers designs used a fixed diffraction grating and a detector array to measure the spectrum [7]. The NIR detector arrays are expensive to manufacture and their cost increases as the number of pixels increases. An alternative is to use a moving diffraction grating and a single NIR detector [8]. This keeps the total cost of the spectrometer low. The diffraction grating can typically be made movable by manufacturing it on a MOEMS micro-mirror.

A typical micro-spectrometer setup is the Czerny-Turner spectrometer [9], shown in Figure 1-1. It uses an Infrared (IR) beam that is passed through the

gas under test where its spectrum is modified depending on the composition of the gas. This beam then passes through an entrance slit before being collimated onto a MOEMS micro-mirror using a concave mirror. The micro-mirror is coated with a reflective grating which diffracts the light before hitting a secondary focusing mirror. As the micro-mirror oscillates the focused light spectrum sweeps across an IR detector. The signal from the detector is digitised into an absorption spectrum which is used to detect the composition of the gas under test using a digital signal processor (DSP).

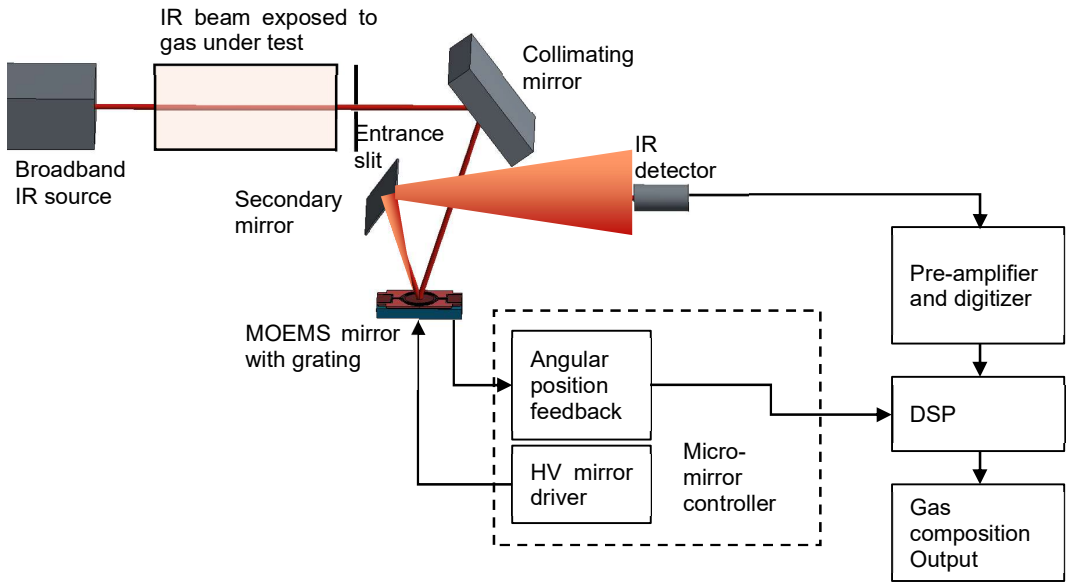

Figure 1-1: Czerny-Turner micro-spectrometer layout

MOEMS micro-mirrors come in a variety of designs each with specific advantages and disadvantages which make them suitable for different applications. The micro-mirror used for this study is a resonating micro-mirror with electrostatic actuation using angular vertical comb structures. Resonating micro-mirrors have the advantage of offering large deflection angles in repeating cycles. This is particularly ideal for micro-spectrometers since the sinusoidal oscillations are used to sweep the diffracted light repeatedly.

Angular vertical comb structures have the advantage of implementing the mirror and actuator on a single silicon-on-insulator layer, thus making them cheaper to implement. A typical angular vertical comb micro-mirror structure is shown in Figure 1-2.

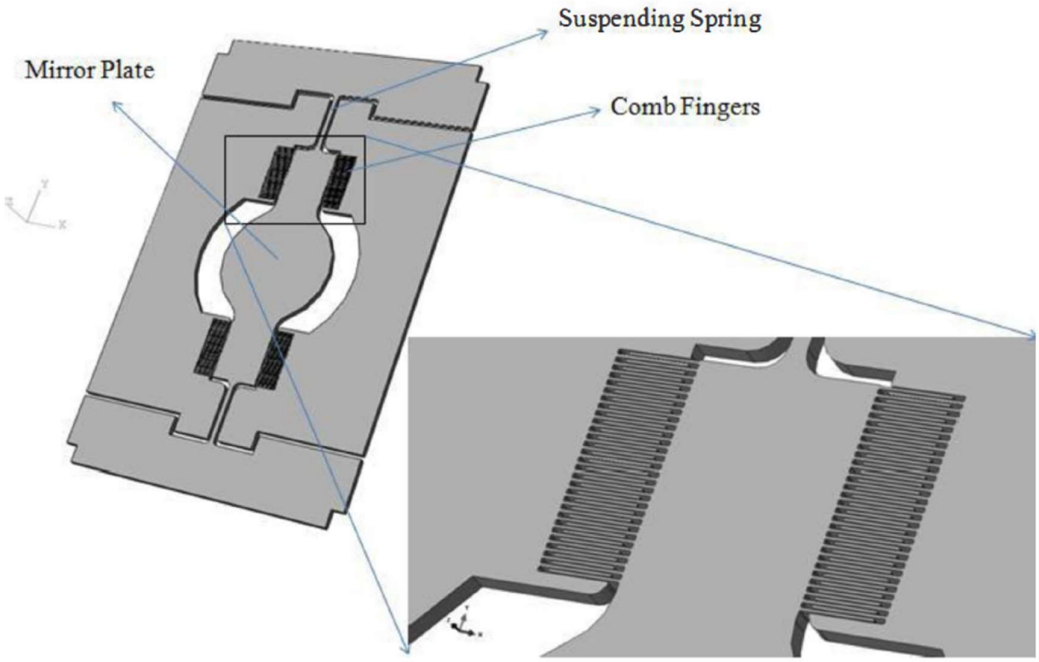

Figure 1-2: Schematic layout of an angular vertical comb micro-mirror, and a close-up of the comb finger region [10]

The work presented in this thesis consists of an analysis and development of a controller for a MEMS micro-mirror within the application of micro-spectrometers. The research focused in designing a low cost and easy to implement controller which integrates a feedback mechanism for stable micro-mirror oscillation amplitude. The controller can also be used in other applications such as lidar-scanner and pico-projectors.

1.1 Motivation

The University of Malta is actively developing a micro-spectrometer aimed at environmental gas detection. This advanced device is designed as a Czerny-Turner micro-spectrometer, which utilizes a resonating micro-mirror to scan diffracted light across a detector. A critical component of this design is the precise control of the micro-mirror, as a stable oscillation amplitude directly impacts the accuracy and resolution of the spectral window being measured. Additionally, real-time feedback on the micro-mirror's position is essential to accurately determine the wavelength being detected.

The motivation for this research arises from the need to enhance the performance of the micro-spectrometer through the development of an advanced micro-mirror controller. This controller not only needs to maintain stable oscillations but also provide precise feedback on the mirror's position to ensure accurate spectral measurements.

Furthermore, the micro-mirror controller designed in this research has broader applications beyond micro-spectrometers. It can be adapted for use in other high-precision optical systems, such as Light Detection and Ranging (LIDAR) scanners, which are crucial for various applications including autonomous vehicles, robotics, and environmental monitoring.

The work undertaken in this research will focus on developing an innovative micro-mirror controller ASIC. This circuit will integrate necessary components such as a high voltage driver and a low voltage digital closed loop controller together with the required feedback configuration, demonstrating its feasibility and effectiveness as a single die implementation. By achieving this, the research aims to contribute significantly to the fields of micro-spectrometry and LIDAR technology, providing a foundation for future innovations and applications.

1.2 Scope

The scope of this research involves the design and manufacture of a micro-mirror controller integrated circuit specifically for use in micro-spectrometers operating with an existing micro-mirror. The micro-mirror available for this study is an angular vertical comb (AVC) drive resonating micro-mirror operating at around 21 kHz: this micro-mirror was chosen due to its stability with respect to resonant frequency and amplitude, as well as ease of fabrication. While the complete spectrometer is being developed by other teams at the University of Malta, this research focuses mainly on the development of a closed-loop controller, improved feedback mechanisms for position sensing, and ASIC integration of a high voltage driver and the low voltage control system. Additionally, the design of the integrated circuit is influenced by the technologies available through Europractice, which the University of Malta is a member of. Cost and simplicity are critical considerations throughout the design and implementation process to ensure feasibility and practical application.

1.3 Aims and Objectives

The main aim of this research is to design, and subsequently characterise fabricated prototypes of, a micro-mirror controller integrated circuit for driving, controlling, and sensing micro-mirror oscillations, specifically for use in micro-spectrometers. Two essential outputs of the ASIC, namely, the amplitude of the micro-mirror oscillation and the phase angle between the driving voltage and mirror angle, serve as inputs for the micro-spectrometer for an accurate spectral wavelength mapping. The ASIC will also integrate the high voltage driver needed to actuate electrostatic micromirrors, demonstrating the feasibility of implementing the controller on a single die.

The research will begin with a detailed analysis of the energy transfer to an angular-vertical-combs (AVC) electrostatic micro-mirror driven by different actuating waveforms. This analysis aims to enhance the understanding of how sine and square waves affect energy transfer to the resonating micro-mirror during operation. With this information, an informed choice on the type of waveform and its phase can be made in order to maximize the amplitude of the mirror oscillations aimed at increasing the spectral window scanned by the micro-spectrometer.

The continuous reduction in CMOS technology linewidth enables compact ASIC implementation of digital logic. Additionally digital implementation allows for development work to be carried through an FPGA environment which facilitates iterative optimisation before transfer to the ASIC. Thus, the micro-mirror controller will be designed and implemented in digital logic. This also allows for ease of subsequent integration of the digital controller with the digital logic of the spectrometer.

A high-resolution frequency synthesizer is needed as part of the control system to drive the micro-mirror at its exact resonant frequency. For a fully digital implementation of the synthesizer, an analysis will be conducted on different types of fractional-N dividers in order to choose the best technique to achieve constant amplitude of micro-mirror oscillations.

Another crucial component of the digital logic for the micro-mirror controller is the feedback mechanism used to detect the amplitude of oscillations and the phase relationship between the applied voltage and mirror angle. This research aims to improve the overall accuracy of these measurements while minimizing implementation costs. This will be achieved by enhancing existing feedback mechanisms that use electrical pulses from photodiodes in the path of a reflected laser beam to measure both amplitude and phase. Improved

amplitude and phase measurements will translate into a more accurate spectral measurement.

One of the aims of this research is to integrate a pulse width modulator within the digital controller in order to adjust the energy transferred to the micro-mirror, thereby controlling the oscillation amplitude. This work also entails an analysis of the effects of shifting the leading or trailing edge of the micro-mirror actuating waveform when modulating the pulse width. Ensuring a linear relationship between the PWM input and amplitude of oscillations means that a simple closed loop controller can be used to achieve stable oscillation amplitude, thus improving the stability of the spectral measurement.

1.4 Thesis organisation

Chapter 2 of this thesis consists of a literature review of work previously carried out on micro-mirrors and their controllers. Chapter 3 focuses on the analysis of micro-mirrors performance for different drive waveforms and design of closed loop controllers. This chapter is divided into five sections: Section 3.2 presents an analysis of the energy transferred to the micro-mirror for different waveforms and the corresponding phase at resonance; Section 3.3 introduces an innovative technique for measuring the phase and amplitude of the micro-mirror; Section 3.4 presents an all-digital micro-mirror signal synthesizer; and Section 3.5 uses the information from sections 3.1 to 3.4 for the design of and analytical model of the micro-mirror controller and its testing using an FPGA implementation; Section 3.6 presents an analysis of the effects of different pulse width modulation techniques on electrostatic micro-mirrors.

Chapter 4 presents the work carried out on implementing the controller on an ASIC, together with accompanying analogue drive circuitry. This implementation demonstrates that the controller can be integrated on a single chip. Chapter 5 presents the results obtained from the ASIC prototype testing.

2 Literature review

This chapter presents a detailed review of state-of-the-art micro-mirror technologies and their control. A detailed description of different means of actuation followed by different ways of controlling the micro-mirror position is presented. This is further elaborated with details of various feedback techniques used in closed-loop control of micro-mirrors. Since the focus of this study is on digital control of micro-mirrors, which requires a high-resolution frequency generator, a detailed description of different types of fractional-N dividers in the use of frequency generation is presented.

2.1 Micro-mirrors

MEMS Micro-mirrors consist of a reflective surface on a moving structure that can be oriented in such a way to steer an incident beam of light. Typical applications include compact projectors, 3D-laser scanners [11], optical switches, scanning spectrometers [12, 13], gas sensors [14, 15], and fringe projection profilometry [16]. The performance of micro-mirrors is typically influenced by the reflective area size, scan angle, operating frequency/response time, and quality factor. Micro-mirrors are typically classified in two groups, resonating and non-resonating. The resonating type makes use of a mass-spring-damper system with an in-phase energy input which builds up oscillations of the reflective surface. On the other hand, non-resonating micro-mirrors make use of larger input torque to overcome the flexure stiffness of the structure and move the reflective surface to a desired steady state position.

Four main actuation principles are typically used: electrostatic actuation, electromagnetic actuation, piezoelectric actuation and electrothermal actuation.

Electrostatic actuation is the most widely used technology since it can be implemented without any expensive compound material and is easily incorporated into the full system. On the other hand, piezoelectric actuation requires piezoelectric material such as PZT while moving coil electromagnetic actuation requires the integration of permanent magnets in the final package.

2.1.1 Electrostatic actuation

Electrostatic angular resonating micro-mirrors are particularly easy to manufacture in standard MEMS processes, since they do not require any specialised material and they can be implemented in a single plane [17]. This type of actuation can be implemented using parallel-plate or comb drive. The parallel plate technique is easy to implement; however, it requires very high actuation voltage and has a limited scan angle. On the other hand, out of plane comb drive actuation was introduced in [18] and consists of two interdigitated rows, one static and one free to move. This allows larger motion in a more compact form factor with a more evenly distributed force over the motion.

Comb drive actuators can be divided in two main sub-categories, staggered vertical combs (SVC) and angular vertical combs (AVC) [12]. SVC are typically manufactured by etching two finger sets in separate device layers in an SOI wafer [19]. This complicates the fabrication process and generally requires different masks for each layer which need to be aligned accurately. SVC are typically used in non-resonating micro-mirrors where a constant torque is required to tilt the mirror to the required angle.

AVC drive are fabricated in a single layer of silicon and are therefore simpler to manufacture and are typically used in resonating micro-mirrors. When operating, a voltage is applied while the change in capacitance is positive thus providing energy into the system. In the initial ideal state, no force is applied to the moving structure when a voltage is applied. For this reason, a small offset

is usually introduced in the system. An example of how to achieve this is by etching a small offset in one side of the comb structure [20]. In some applications the process variation and surface deformation during the manufacturing process can be enough to produce sufficient offset in the system.

AVC drive has been extensively modelled using analytical and FEA analysis. This type of drive consists of intertwined comb structures as shown in Figure 2-1. As the comb structures disengage, the capacitance changes nonlinearly, thereby introducing a non-linear component into the mirror model [21]. Further non-linearities are introduced due to mechanical spring stiffening [22], electrostatic spring softening [12], and the non-linear damping characteristics of the mirror [23]. This non-linearity can introduce a hysteresis in the frequency response plot.

Designing electrostatic micro-mirrors requires careful consideration of lateral instability, which can significantly impact performance. Lateral forces may escalate at high voltages due to factors such as alignment accuracy and etching process errors. Any imbalance in the lateral forces on the left and right sides of the vertical comb-drive structure can lead to instability, resulting in contact between the movable and fixed comb fingers [24]. This contact triggers lateral adhesion, which hinders performance and can lead to device failure. Therefore, ensuring precise fabrication and addressing potential lateral instabilities during the design phase is crucial for reliable micro-mirror operation.

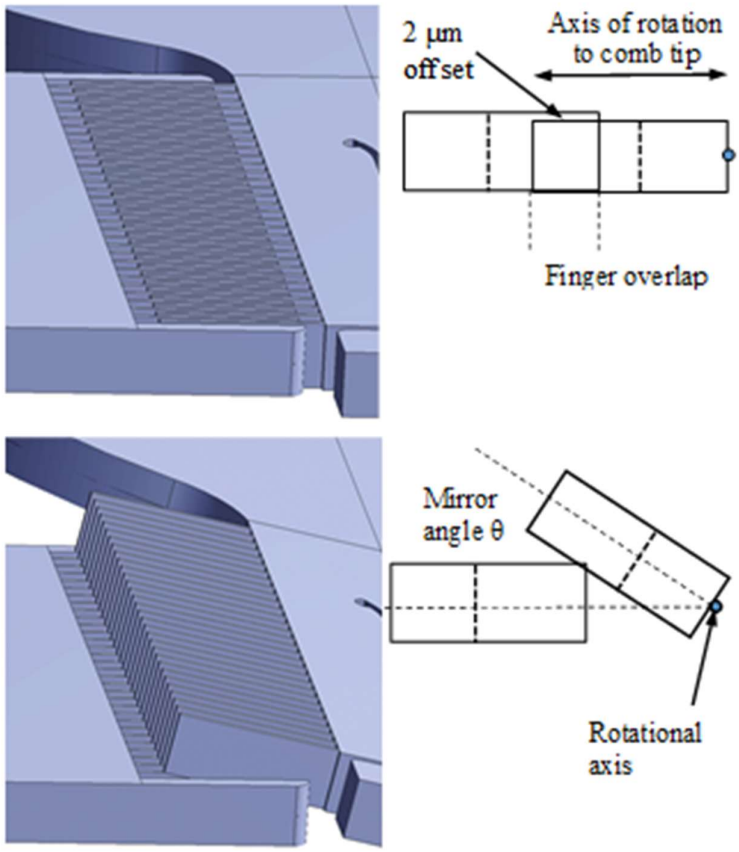

Figure 2-1 Typical vertical comb-drive used for resonating micro-mirrors. Top: stationary (angle = 0), bottom: mirror at angle θ.

2.1.2 Electromagnetic actuation

Electromagnetic actuated micro-mirrors can be implemented in two ways: moving magnet, or moving coil. The moving magnet scheme uses a micro-mirror with a bulk magnet, or a thin film deposited magnet on the moving structure and a set of stationary coils. The moving structure is simple to manufacture since is does not require any electrical contacts. In the moving coil scheme, a coil is embedded in the moving micro-mirror and a set of external magnets on the sides provide a static magnetic field [25]. This type of actuation is more linear compared to other techniques and can be implemented for dual-axis micro-mirror, which are typically required for LiDAR applications [26].

Electromagnetic actuation requires high current though the drive coils. This causes high thermal dissipation which can be difficult to manage in micro-devices. Moreover, magnets strong enough to operate the micro-mirror to the desired amplitude can be bulky and might require magnetic shielding which further increases the size of the final package.

2.2 Micro-mirror control

Precision control of the mirror oscillating frequency and amplitude is important in certain applications. For example, in the application of micro-spectrometers, variations in the amplitude and frequency result in a change in the optical spectral window. These changes can lead to a loss in spectral accuracy. Several control techniques have been proposed in order to control the resonating micro-mirror. These include: open loop control, where the system forward transfer function is used to adjust the drive voltage in order to obtain the required amplitude [27, 28]; and closed loop control, where a feedback mechanism is used to sense the mirror position and adjust the drive voltage [8, 29]. A common technique in closed loop mirror control is to use a Phase Locked Loop (PLL) in order to operate the mirror at its resonant point [30, 31]. Since the mirror is operating at its resonant point, the maximum possible amplitude can be obtained for a limited applied voltage.

2.2.1 Open loop control

Open loop control of a MEMS device has been demonstrated in various publications. This has the advantage of not needing additional sensing devices and generally relies on having an accurate model of the MEMS device [32].

A common technique in open loop control of MEMS devices is input signal shaping. By carefully modifying the drive signal to the actuator, the vibration induced by motion can be significantly suppressed [33]. This type of control is

ideal in applications where point-to-point motion is necessary, such as non-resonating micro-mirrors [34].

Several techniques are available for shaping the drive signal to obtain the required system response. In [27] two techniques are compared for shaping the drive voltage with the aim of reducing the oscillations of a two-axis non-resonating micro-mirror. The simplest approach discussed uses an adequate low-pass filter to prevent excitation of the resonance mode. A more precise approach uses inverse-square-root to invert the device model and compute the optimal input waveform with system bandwidth limitations represented by a low pass filter. Both approaches show adequate system response for the device used by the authors, where the non-linearity derives from the electrostatic actuation force relationship.

Other proposed techniques for input shaping of micro-mirrors include: limited jerk trajectories for reduction of residual oscillations [35], trajectory planning and robust non-linear control based on differential flatness of the mirror response [36], and by using energy conservation, force equilibrium, elliptical integral computation [37], and double step control method [38].

The main drawback of open loop control is the lack of compensation for system changes over the lifetime of the sensor. These changes include performance changes depending on ambient conditions such as temperature and humidity. The performance of the micro-mirror can also change over system operating hours due to micro-cracking that can build up in the springs.

2.2.2 Closed loop control

While open loop techniques can be used to operate micro-mirrors, they cannot compensate for model inaccuracies or external disturbances, such as long-term parameter drifts due to temperature and pressure changes. The basis of closed loop control is the integration of a feedback mechanism that relays back the

current operating condition of the actuator. The controller then uses the error between the measurement and desired output to correct the micro-mirror drive signal.

Several techniques have been proposed in literature for measuring the mirror position.

2.2.2.1 Separate set of Comb-fingers - capacitive

The simplest way to measure the instantaneous position of the micro-mirror is to add a capacitive sensor on the MEMS device. This is usually done by adding another set of comb fingers next to the drive structure [39]. This technique has been used in several other applications such as accelerometers [40] and has been extensively analysed.

The most common way of measuring change in capacitance is to apply a DC voltage across the capacitor and then measure the current produced when the capacitance changes. This usually requires a high voltage to maximize the current generated. The applied voltage will also exert a force on the system which usually results in electrostatic spring stiffening.

An alternative is to measure the capacitance using a high frequency impedance analyser [31]. In this approach a high-frequency constant-voltage signal is applied to the sensing comb. The current is then sensed and demodulated in order to generate a signal which is proportional to the sensing capacitance. In this case, using a higher frequency results in a higher current which can result in a better signal to noise ratio. The high-frequency sense signal can also be superimposed on the drive signal, and a single set of drive and sense comb structures are used [41]. However, this limits the system to using sinusoidal drive signals only.

The main disadvantage of this approach is the addition of a secondary structure on the micro-device. This will increase the size of the device and thus increase its cost.

2.2.2.2 Current sensing

An alternative to the previous method is to use the drive comb structure for both actuating the mirror and sensing the mirror position. This is commonly done by measuring the drive current in the actuating circuitry [42]. Since the voltage is not constant, measuring the mirror position from this current is not trivial. The instantaneous current produced in the drive comb is defined by the equation (1); where i is the drive current, C is the comb structure capacitance, $\frac{dv}{dt}$ is the rate of change in capacitance, V is the drive voltage, and $\frac{dC}{dt}$ is the rate of change of capacitance:

$$i = C\frac{dv}{dt} + V\frac{dC}{dt} \tag{1}$$

This equation can be complex to solve for the situation where a sinusoidal voltage is applied to the micro-mirror. In the case of square wave drive, the $C\frac{dv}{dt}$ term will be zero for the flat parts of the waveform [43]. Masking during rising and falling edges is usually used to remove this part of the equation [44].

2.2.2.3 Optical Sensing using PSD

A position sensitive detector (PSD) is a photodiode with multiple tabs which can be used to measure the position of a laser spot in relation to its centre. If a laser beam is reflected off the micro-mirror and onto a PSD, the position of the mirror can be measured [45]. PSD sensors can be bulky and are generally used in lab applications where precise and repeatable measurement of the micro-mirror angle is required [27].

2.2.2.4 Quadrant detector scheme

An integrated option using an optical feedback mechanism was proposed in [46]. In this approach the back side of the micro-mirror is illuminated using an external light source. The reflected light is detected using four photodiodes placed at the four corners underneath the mirror.

A depiction of the setup is shown in Figure 2-2. The detector axes are set at 45° with reference to the axes of rotation of the mirror. The equations below can then be used to determine the mirror angle.

$$RDI_X = \frac{(I_{NW} + I_{SW}) - (I_{NO} + I_{SO})}{I_{NW} + I_{SW} + I_{NO} + I_{SO}} \quad (2)$$

$$RDI_Y = \frac{(I_{NO} + I_{NW}) - (I_{SO} + I_{SW})}{I_{NW} + I_{SW} + I_{NO} + I_{SO}}.$$

where RDI_x and RDI_y are the relative differential intensity along the x and y axis, respectively, and I_{NW}, I_{SW}, I_{NO}, and I_{SO} are the intensity signals from the individual photodetectors [46].

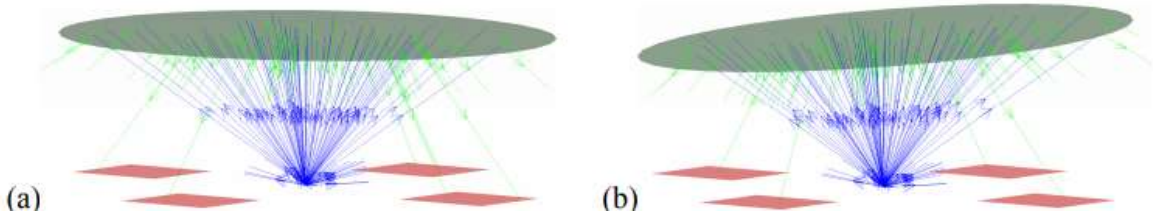

Figure 2-2: Schematic of the quadrant detection scheme. (a) mirror at zero deflection (b) mirror with 5° deflection [46]

From the equation it can be noted that the system has a linear relationship between the mirror angle and the output and there is no cross talk between the two axes. This is true for the situations where all four detectors are illuminated,

and the backside of the mirror is larger than the aperture between the four detectors.

In [46] this scheme was tested in two ways, the first using four separate detectors mounted on a PCB and mounted under micro-mirror, and the second using a four-quadrant diode with a centre hole mounter under the micro-mirror. The authors estimate an error of one degree for the first setup and 0.3 degrees for the second setup. The results of this technique are shown in Figure 2-3.

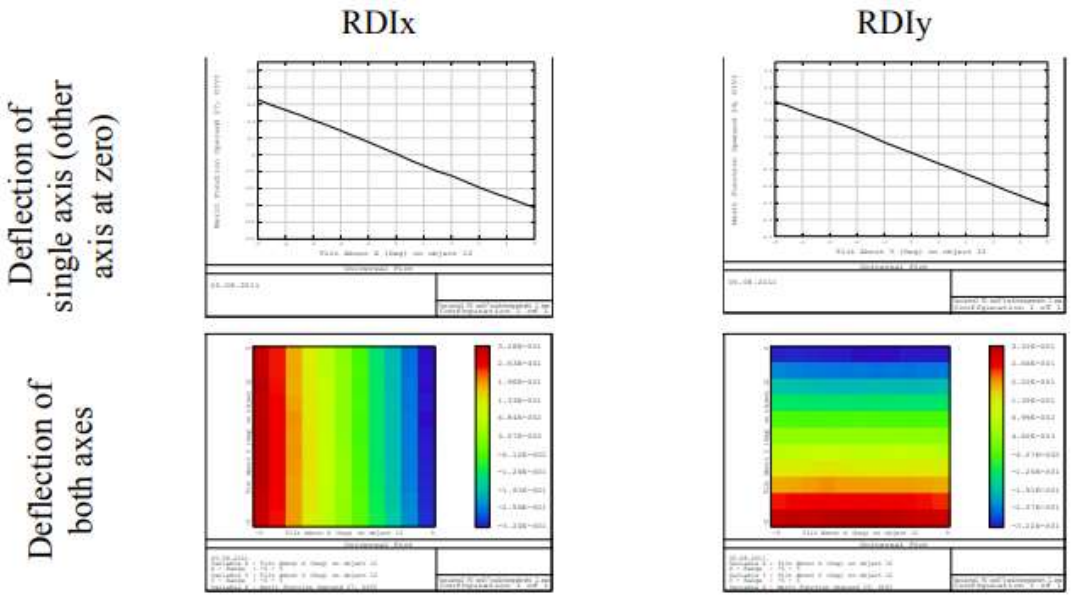

Figure 2-3: Position signal as a function of deflection angle for a two axis micro-mirror [11]

2.2.2.5 Photodiode pulse timing-based amplitude and phase measurement

An optical feedback technique for resonating micro-mirrors originally introduced in [47] and further described in [48] and [49] consists of placing two photodiodes in line with a laser beam reflected off the micro-mirror. The angular position of the mirror is then calculated using pulse timing and a harmonic extrapolation function. Placing one of the photodiodes at zero

deflection angle allows accurate timing of the zero transition. The second diode is positioned at a known deflection angle and is used to determine the oscillation amplitude.

The setup used in [48] is shown in Figure 2-4a. The beam is reflected off the back of the micro-mirror so that it does not interfere with the optics installed at the front side. Figure 2-4b shows the pulse timing generated by the two photodiodes. The mirror phase can be calculated using the following equation:

$$\varphi = \frac{\mathrm{pd}}{T} 360^{\circ}. \tag{3}$$

where φ is the phase of the micro-mirror, pd is the delay between the falling edge of the driving voltage and the mirror zero transition, and T is the oscillation period.

The amplitude of the oscillations, A, can be calculated from equation (4), where X_0 is the position for the second photodiode and t_A is the timing defined in Figure 2-4(b).

$$A = \frac{X_0}{\sin(\pi((1/2) - (t_A/T)))}. \tag{4}$$

The position of the second photodiode determines the minimum angle that can be measured and thus minimum angle where the mirror oscillation amplitude can be controlled. It is also advantageous to have a larger X_0 as this will improve the accuracy of the amplitude measurement. A trade-off is needed when positioning the second photodiode to achieve good accuracy while being able to measure the amplitude of oscillations at low angle.

The second photodiode can also be used to determine unequivocally the direction of oscillation, which is not directly evident from first photodiode

signal alone. This is because the initial deflection of the mirror is arbitrary at each start up.

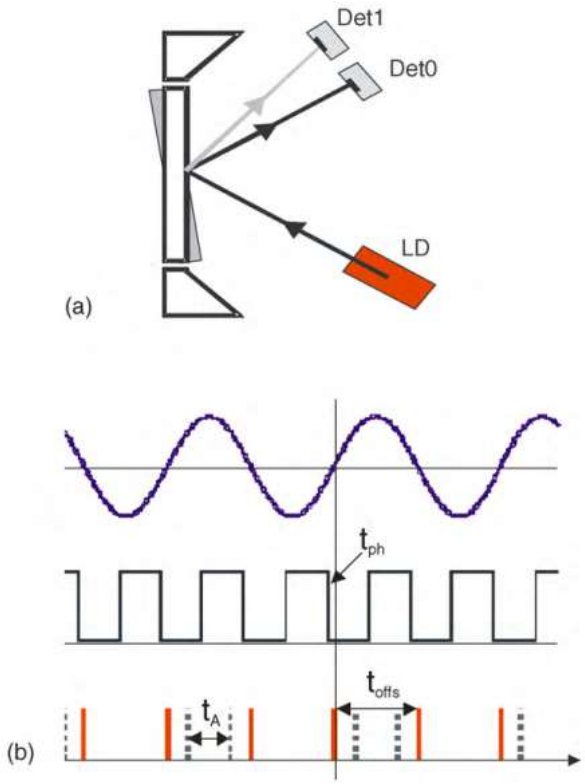

Figure 2-4: Scheme of the optical sensing principle presented in [49]: (a) optical layout (b) relevant signals. From top to bottom: mirror position, drive signal, photodiodes signals

2.2.2.6 Piezoelectric and piezoresistive feedback

Piezoelectric feedback involves using piezoelectric materials to generate an electrical signal in response to mechanical deformation. In micromirrors, this technique enables precise control over the micromirror angle by converting mechanical displacement into an electrical signal, which can then be used for closed-loop control [50]. Piezoelectric materials, such as lead zirconate titanate (PZT) are often employed for their high sensitivity and ability to operate over a wide frequency range [51].

Piezoresistive feedback, on the other hand, uses materials whose electrical resistance changes when subjected to mechanical stress. This method involves embedding piezoresistive sensors in the micromirror structure to measure the strain or deformation of the mirror. The change in resistance is then converted into an electrical signal for feedback purposes [52]. Piezoresistive sensing is known for its linear response and stability over a range of temperatures. The two techniques can also be combined to improve system stability [53].

2.2.2.7 Phase control of resonating micro-mirror

To obtain the maximum oscillation amplitude in the micro-mirror for a given maximum voltage, the mirror should be operated at its resonant frequency. This frequency is not always equal to the natural frequency of oscillations due to damping factor and electrostatic spring stiffening.

The most common technique for operating MEMS resonating structures is to use the direct amplification method: frequency locked loop (FLL) or a Phase locked loop (PLL) [54]. In both cases the controller output frequency is adjusted depending on the measured frequency or phase of the micro-mirror. While in certain applications, such as in dynamic force microscopy, the FLL was shown to be superior to the other methods [55], it is also more complicated to implement and the phase difference is dependent on the initial conditions of the system [56]. Both the PLL and FLL can be implemented in an all-digital circuit. The micro-mirror non-linear response with frequency, which includes a non-continuity and hysteresis [23] means that the FFL is prone to unstable operation.

A phase locked loop has good phase and frequency control of MEMS micro-mirrors and can be implemented in analogue or digital circuitry. The analogue approach can achieve high timing resolution; however, it requires complicated circuitry and does not allow for the implementation of complex control

algorithms. The digital approach is easier to implement but requires high clock speeds to resolve timing signals with high resolutions [48]. Digital asynchronous PLL (DAsPLL) is an alternative to digital PLL which can achieve fast and precise phase tracking without the need of high-speed clock [44].

2.2.2.8 Micro-mirror amplitude control

Amplitude control is an important factor in micro-mirror devices. This is especially important in micro-spectrometers since any change in amplitude results in a shift in the spectral response [8]. Open loop operation would not be possible since any variation in environmental conditions (such as temperature and humidity) will also affect the amplitude of oscillations.

A technique for controlling the amplitude of a micro-mirror is to change the amplitude of the drive signal. This can be achieved by using a variable gain amplifier (VGA) which is controlled by an error signal generated by comparing the measured amplitude of oscillation with a reference signal [8]. An alternative is to use a PWM signal with a frequency higher than the drive frequency [57]. The approach generates an adjustable amplitude signal which can be driven directly by the digital closed loop controller.

Another approach is to use phase control of the micro-mirror. In this method, the phase of the drive signal and the mirror angle are varied to modulate the energy transfer to the system. This technique has been demonstrated to be effective in electromagnetic micro-mirrors [58].

2.3 All digital high-resolution frequency synthesis

Resonant micro-mirrors manufactured in silicon have a high-quality factor which results in a narrow operation bandwidth. This means that signals with a

high frequency precision are needed to operate them, which are difficult to achieve when using all-digital integer dividers.

A common technique to obtain a high frequency resolution is to use a voltage-controlled oscillator together with a digital-to-analogue converter. This introduces a further complication as both analogue and digital circuitry would be required. An alternative is to use a Direct Digital Synthesizer (DDS) together with a digital fractional-N divider to generate a precise frequency. This type of divider alternates between two frequencies, generated by integer dividers, in order to create an averaged frequency. An improvement over the fractional-N divider is the delta-sigma fractional-N divider [59]. This divider uses a delta-sigma modulator to randomly distribute in between the two integer divisions. Another alternative is the dithering technique [60], where unlike the previous two methods, the window in which the two frequencies alternate changes depending on the output frequency. This approach is also simpler to implement in digital logic [61].

2.3.1 Integer divider frequency synthesizer

A typical digital frequency synthesizer consists of a reference clock source F_R, an output frequency F_O, and a control signal N as shown in Figure 2-5. The output frequency is set by equation (5).

$$F_O = \frac{F_R}{N} \tag{5}$$

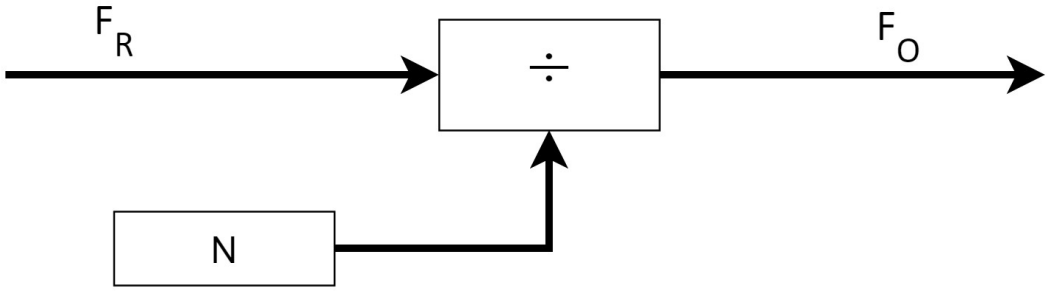

Figure 2-5: Integer divider frequency synthesizer

The minimum frequency resolution, or minimum channel Fs spacing, is defined by equation (6)

$$F_S = \frac{F_O}{N} = \frac{F_R}{N^2} = \frac{F_O^2}{F_R} \tag{6}$$

Resonating micro-mirrors have a high-quality factor and therefore narrow bandwidth, typically 20 Hz with a resonant frequency of 21 kHz. This means that high frequency resolution is needed to operate at its resonant point. Such high resolution is difficult to achieve using integer dividers since a very high reference frequency would be required.

2.3.2 Fractional-N Divider

Fractional-N dividers offer superior frequency resolution compared to integer dividers. This type of frequency synthesizer alternates between two integer divider values to achieve an average output frequency that lies between the outputs of the individual dividers [62].

A typical layout of fractional-N divider is shown in Figure 2-6. Similar to the integer divider setup, a signal with frequency F_O is generated by dividing the reference source frequency F_R with a divisor value which is alternated between N and N+1 with a ratio of B/C. This alternation effectively creates an average divisor value, allowing for finer frequency resolution than fixed integer

dividers. The resultant output average output frequency is defined by equation (7).

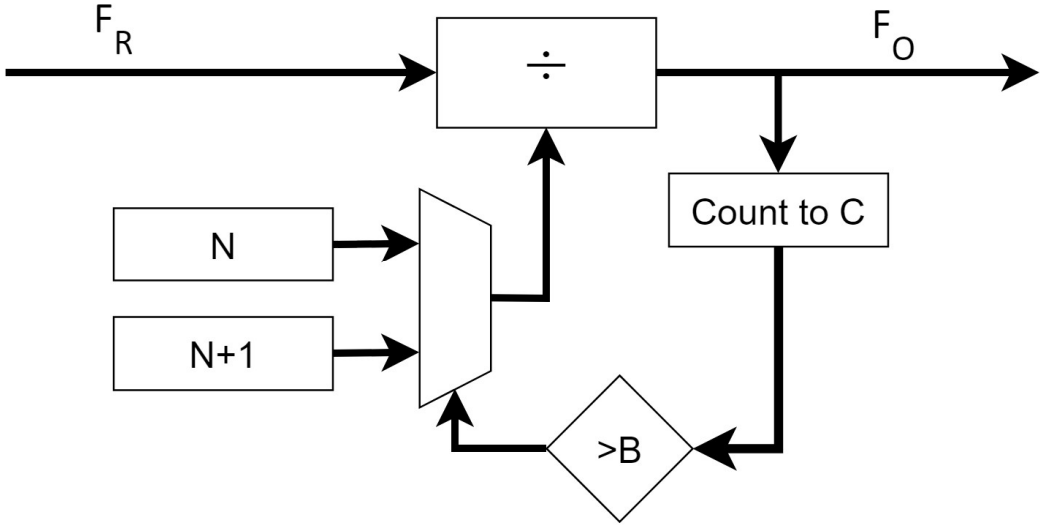

Figure 2-6: Fractional divider frequency synthesizer

$$F_O = \frac{BF_R}{C\ N} + \frac{(B-1)\ F_R}{C\ (N+1)} \tag{7}$$

While the average output frequency is constant, the instantaneous output frequency is modulated between two frequencies, resulting in side bands in the frequency response. These side bands, also called spurs, can have a considerable amplitude when compared to the total output signal. If the spurs are within the bandwidth of the micro-mirror, they can introduce perturbation in the mirror's oscillation amplitude.

2.3.3 Delta-Sigma Fractional-N divider

A method for reducing the spurs in fractional-N dividers is to use a delta-sigma fractional-N divider. Similar to the previous approach, a divider with a division value of N or N+1 is used; however, instead of using a timing window to choose between the two divisions, a delta-sigma modulator is used. A block diagram

of the system is shown in Figure 2-7. The output resolution is the same as the fractional-N divider approach.

This approach randomly distributes between the two integer divisions, which means that the spurs are shifted away from the centre frequency. This makes them less likely to affect the system during operation [63].

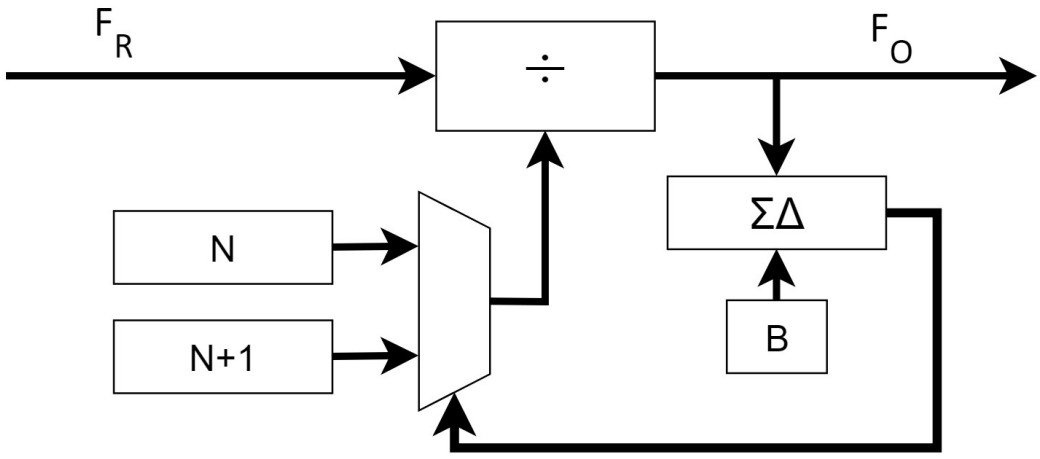

Figure 2-7: Delta-sigma fractional divider frequency synthesizer

2.3.4 Dithering technique

An alternative to the delta-sigma fractional-N divider is the dithering technique presented in [60]. The system is again switching between two integer division in a pseudo random pattern; however, this approach does not use a fixed window width. Instead, the period between repeating cycle changes depends on the output frequency.

This is achieved using the procedure shown in Figure 2-8. The system uses a counter which is accumulated in steps of size S with every input clock cycle. When the size of the counter is larger than the target T, the target is subtracted from the counter and the output toggled. This means that at the start of the next cycle the counter contains the overflow of the previous cycle. The overflow adds up over each cycle until it becomes bigger than the step size. In this case

an extra step is needed for overflow to occur and thus making the cycle longer and the overflow smaller than the step size.

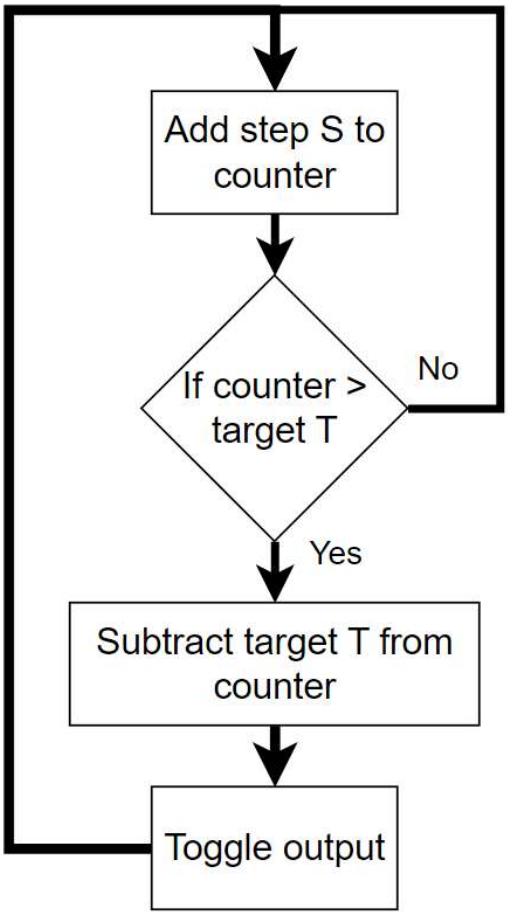

Figure 2-8: Dithering technique flow chart

$$F_O = \frac{S\,F_R}{2\,T} \tag{8}$$

Using this technique, the frequency resolution is defined by the equation below:

$$F_S = \frac{F_O}{T} \tag{9}$$

This means that the resolution is increased by the value of S when compared to integer dividers.

2.4 Review summary

The literature review described here is used as the basis for the research in the following chapters. The introduction to different types of micro-mirrors with focus on AVC micro-mirror is used as the starting point in the analysis of the micro-mirror drive characteristic. This is done with the aim of maximising the micro-mirror oscillation amplitude for a limited maximum voltage.

An analysis of previously published micro-mirror control techniques and their respective feedback mechanisms has been presented in this chapter. Knowledge obtained from this part of the literature review is used in this study for the development of an improved feedback mechanism. The design published in [49] which uses two photodiodes in order to measure both the amplitude and phase of the micro-mirror oscillations is used as the starting point in the design of a simpler setup which uses a single photodiode. The gathered information on control algorithms is then used in the design, simulation, and implementation of a closed loop control.

As part of the implementation of the controller on an FPGA, a fractional-N divider is needed. An analysis on three different types of digital high-resolution frequency synthesis has been presented in Section 2.3. Their performance in driving the micro-mirror is evaluated and reported in Chapter 3.

2.5 Research Methodology

The research project was divided into a number of tasks as shown in block diagram in **Error! Reference source not found.**. A literature review was first carried out on state-of-the-art resonant micro-mirrors and their control. Different types of resonating micro-mirrors, including electrostatic, piezoelectric, and electromagnetic were reviewed together with their various actuation and feedback mechanisms. The most widely used micro-mirror is the

resonating electrostatic micro-mirror and this research work was carried for use with this type of micro-mirror. Once the type of micro-mirror was decided on the next step carried out was an analysis of the drive signal requirements. These drive characteristics include the waveform and its timing relative to mirror position in order to optimise the oscillation scan angle. In a resonating micro-mirror, energy is transferred to the mirror in pulses during each oscillation.

The first part of the research investigates the energy transferred into the system during each cycle for different types of driving waveforms. From the results for the chosen waveform, that is, a filtered square wave, the optimal phase between the applied voltage and the micro-mirror angle was then determined.

Publicly available open-loop and closed-loop controllers, together with feedback techniques used when measuring the mirror position, were then studied. A particular feedback technique uses pulses from a photodiode in the path of a reflected laser beam to measure the phase of the micro-mirror [46]. This feedback technique is used here as a starting point in the design of both scanning angle amplitude and phase measurement technique. In order to produce a more accurate timing measurement an improved pulse edge detection algorithm is developed. The increased timing accuracy achieved allows for a more accurate calculation of the micro-mirror oscillation angle. The simpler hardware translates to a lower implementation cost.

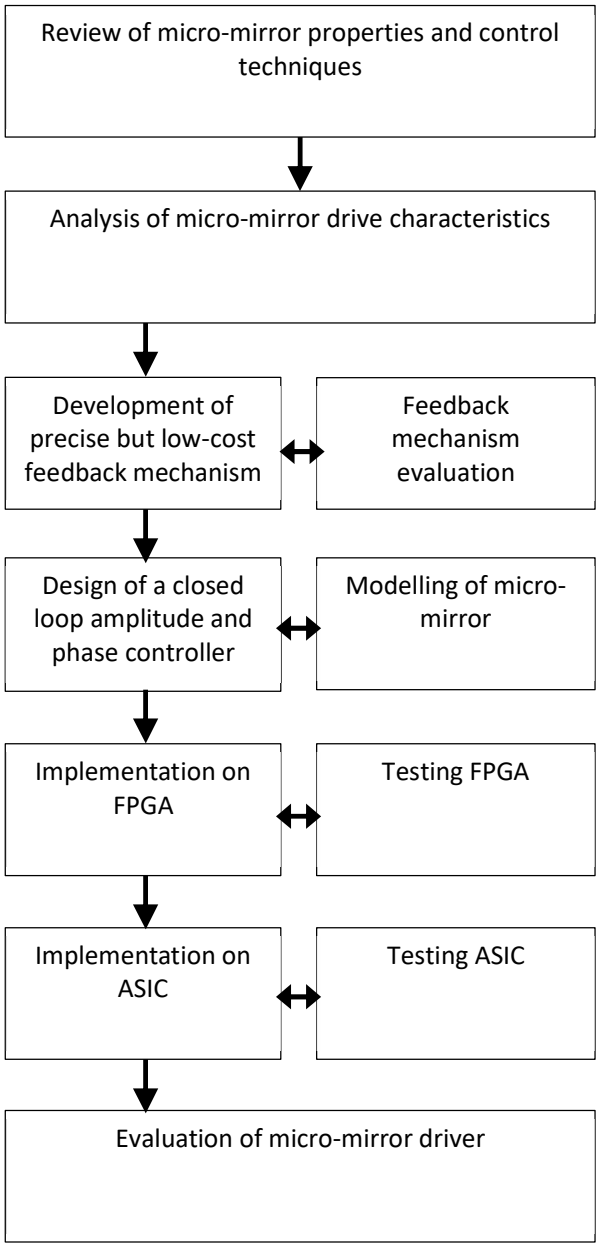

Figure 2-9: Project overview block diagram

A phase locked loop is typically used in resonant micro-mirrors to set the drive frequency. This can be done since at resonance, the phase between the micro-mirror angle and applied voltage is constant. A common approach is to use an analogue phased locked loop [64]; however, with the advancement of digital IC

design, an all-digital implementation can be smaller to implement and more cost effective. A limiting factor in digital phase locked loops is that with integer-N-dividers the output frequency resolution cannot be high enough to operate the micro-mirror within its narrow bandwidth. A solution is to use fractional-N dividers which toggle between two adjacent N-dividers to increase the resolution. However, it is shown in this work, that the toggling of the output frequency resulting from the fractional-N divider, produces small periodic fluctuations in the micro-mirror oscillation amplitude. This can be mitigated with the use of delta-sigma fractional-N dividers which randomize the toggling and therefore reduce the oscillation wobble. However, this would increase the complexity of the digital circuit. An alternative technique, which is more compact to implement, is the dithering technique, which was previously demonstrated as a fractional-N divider for communication purposes [60]. The applicability of this technique as a frequency synthesis method for micro-mirror excitation is investigated here with effective results.

An analytical model of the micro-mirror with the digital phase locked loop was developed using MATLAB. This allows for verification that the feedback mechanism and the phase locked loop are an effective way to operate the micro-mirror.

Apart from controlling the oscillation frequency, some applications such as micro-spectrometers require accurate control of the amplitude of oscillations. This can be achieved using various techniques. In this research it is demonstrated that changing the duty cycle of the driving signal is an effective and simple way to change the micro-mirror oscillation amplitude. The change in duty cycle can be achieved by either shortening the pulse from the front or from the back. It is shown here that by shortening the pulse from the front, a much more linear response is achieved from 0° to 45° of phase.

The phase and amplitude measurement system, the phase locked loop with dithering based frequency generator, and the amplitude control using varying duty cycle were implemented on an FPGA for testing. This enabled testing and verification of individual sections.

While FPGAs are an effective way of testing digital logic, they are typically not used in the consumer products because of their high cost. The alternative is to implement the logic in an ASIC, which is expensive at low manufacturing volume but becomes significantly cheaper when manufactured in high volume. This would be useful considering a trend of incorporating spectrometers in commercial portable devices such as Bruker Opus Touch or the Jsaco VIR-300 NIR Spectrometer. An ASIC implementation is also typically smaller in size and requires a simpler spectrometer PCB since analogue circuitry can be integrated within the same chip. As a demonstration of the practicality of implementing the micro-mirror controller, the digital part and the high voltage amplifier were implemented on one ASIC. The implementation is divided into multiple modules for testability purposes. By implementing the circuit on a process that integrates both the digital logic and high voltage analogue driver on the same integrated circuit, it is demonstrated that the controller and the high-voltage amplifier analogue circuit can be implemented in a single chip. This reduces the PCB area that would be required enabling a more compact micro-spectrometer implementation.

The ASIC was manufactured through Europractice, an E.U. consortium that offers multi-project wafer manufacturing for academic institutions at reasonable cost. Sharing the wafer between multiple users means that the cost of prototyping is considerably reduced per user. An X-Fab SOI process [65] was used since it was the only process available on Europractice that allowed the integration of the digital logic and high voltage analogue modules on the same chip.

All the testing of the various components of the micro-mirror controller was carried out at the University of Malta MEMS characterization facility. In the designed test setup, the micro-mirror angle was continuously monitored using a position sensitive detector, whose output was used to verify the performance of the IC module under test. After fabrication and wire bonding, the ASIC was tested on the same setup, where it was verified that the implemented controller operated with the same precision in amplitude and phase control as that achieved with the FPGA implementations.

This research demonstrates a micro-mirror controller that uses innovative techniques to control the drive waveform and the oscillations' phase and amplitude. It is shown that the controller can be fully integrated in an IC; this can be used in the development of a low-cost high volume hand-held spectrometer.

As an emerging technology, resonating micro-mirror-based micro-spectrometers are still in the developmental stage. This research addresses a critical gap in micro-mirror control technology: the precise control of the micro-mirror's amplitude and phase. This precision is essential for the accurate functioning of micro-spectrometers. Improved accuracy in controlling the micro-mirror's angular position and phase is crucial for better discrimination between different measured spectra, thereby enhancing the spectral resolution of the micro-spectrometer.

By enhancing the understanding of the effects of the drive waveform on a micro-mirror and developing improved feedback mechanisms, this research aims to advance amplitude control and closed-loop system models. Additionally, current high-precision control systems are not available in a compact, low-cost solution. This research fills this gap by designing, implementing, and testing a compact all-digital controller that offers improved precision over previous techniques.

3 Resonant micro-mirror electrical characterization and control

This chapter starts with an analysis of the interactions between electrostatically driven micro-mirrors and their control systems. Different drive waveforms and their respective optimal phase are analysed by investigating the energy transferred to the micro-mirror. This is followed by an evaluation of the different feedback techniques and control strategies compatible with the optimal waveform. This led to the selection of the optimal drive waveform and optimal feedback techniques. For this selected system, an analytical model is implemented in a numerical package and evaluated. Empirical testing is then carried out of the digital implementation of the control and feedback strategies using an FPGA and some feedback hardware. Finally, the FPGA test results are presented.

3.1 Amplitude and phase control of a micro-mirror

The commonly used waveforms (sine, square, BW limited square) are analysed for the amplitude transfer function achieved by each for resonant micro-mirrors. Non-linear operation due to the physical properties of the comb-drive structures used for electrostatic driving is considered in this analysis. The optimum phase for maximum energy transfer is also found. Both the amplitude transfer function and the maximum energy transfer are important for achieving as large as possible actuation angles while minimizing drive voltage and maintaining stable closed loop control using a PLL. These three goals allow for a much more practical implementation of micro-mirrors in real-world systems.

For a successful implementation using a PLL both phase and amplitude information are essential, so a measurement system based on [48], with improvements, is proposed, implemented and evaluated. Contrary to [48] where only phase was measured, both phase and amplitude are here measured accurately by the proposed system. Another advantage of the proposed system is the use of only one single photodiode detector in the path of a reflected laser beam.

Amplitude control techniques which are suitable for fully digital implementation are considered and evaluated for linearity. The goal for a fully digital implementation is to avoid the complexity introduced by existing hybrid solutions which require, in addition to the digital part, various oscillators and DACs [31]. The analogue stages can be affected by manufacturing variation and may increase die area when compared to all-digital implementation.

The proposed micro-mirror control strategy was evaluated using time-domain numerical analysis to ensure its validity prior to physical implementation. Simulation was performed using MATLAB and both start up behaviour and steady state operation data were collected for comparison to empirical results.

Following satisfactory validation, the control strategy was implemented on FPGA hardware together with a discrete photodiode detector and a commercial micro-mirror [66]

3.2 Comparison of electrostatic mirror drive waveforms

The micro-mirrors used for this research use the angular vertical comb drive mechanism shown in Figure 3-1. The image illustrates the structure of a micro-mirror system with fixed and movable comb fingers, including both actuation and sense combs, and highlights the rotational axis around which the mirror

pivots. The torque-voltage relationship using electrostatic actuation via AVC is non-linear and is dependent on the applied waveform and the instantaneous oscillation amplitude.

The micro-mirror used in this study [66] is etched out of silicon and covered in gold. It consists of a 1 mm disc suspended on two torsional springs. On either side of the spring, there is a 31 fingered comb structure having an overlap of 152 μm, a comb thickness of 50 μm, and a comb spacing of 5 μm. The structure is actuated by applying a voltage between the four stationary comb structure (stator) and the mirror structure (rotor). An image of the micro-mirror with a central circular 1 mm mirror, surrounded by actuating comb structures and electrical contact pads at the corners, is shown in Figure 3-2.

A common approach to driving AVC is using a sinusoidal signal with the same frequency as the mechanical resonant frequency of the mirror. Small inaccuracies in the manufacturing process result in the comb structure being slightly offset which results in a small electrostatic force in the structure. This force starts deflecting the structure and thus introduces energy into the system and an oscillation is induced. As the mirror oscillates, the maximum deflection distance between the comb structures increases resulting in increased torque being applied to the system. The phase between the applied voltage and mirror angle automatically settles to a point of maximum energy transfer. Oscillation amplitude stops increasing when the maximum energy transferred to the system in each cycle is equal to the damping losses per cycle.

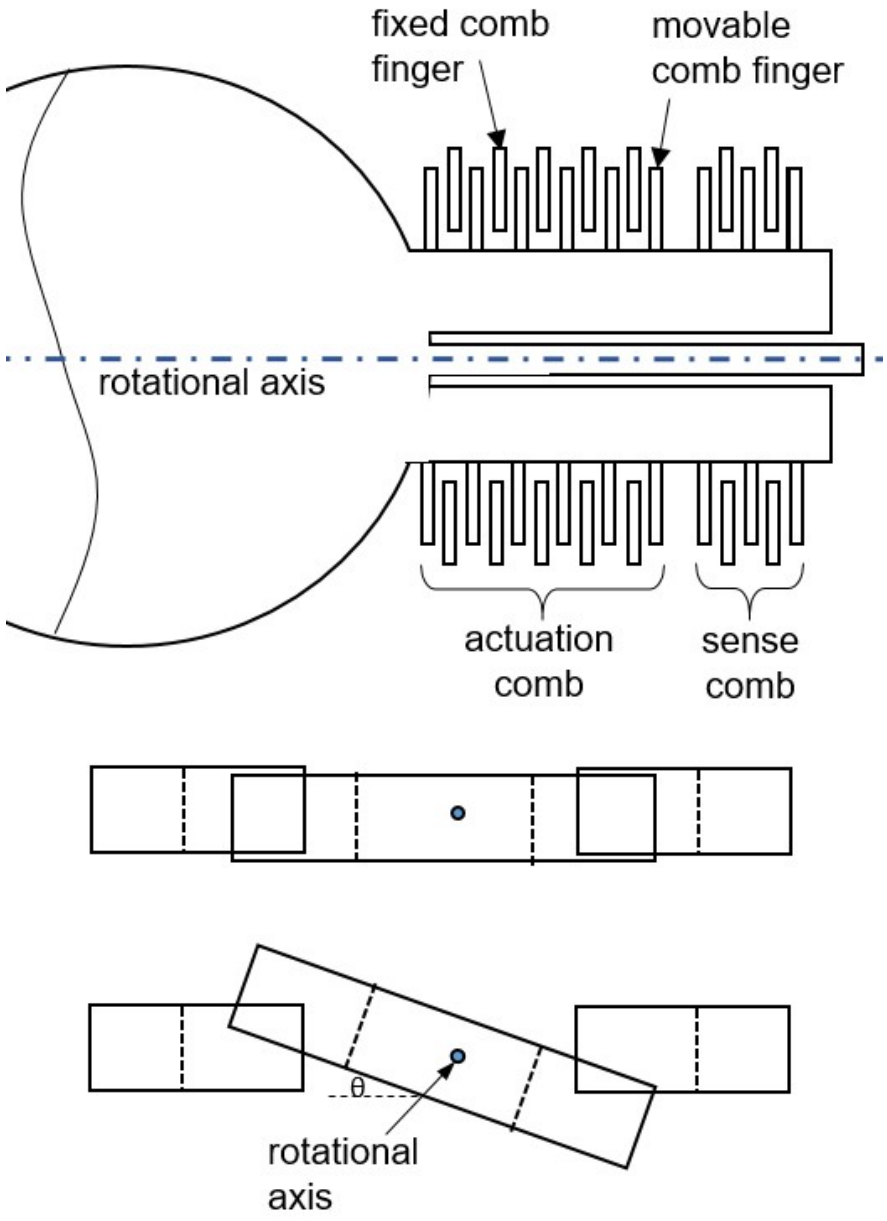

Figure 3-1: Resonant electrostatic mirror layout (top) and cross-sectional view(bottom)

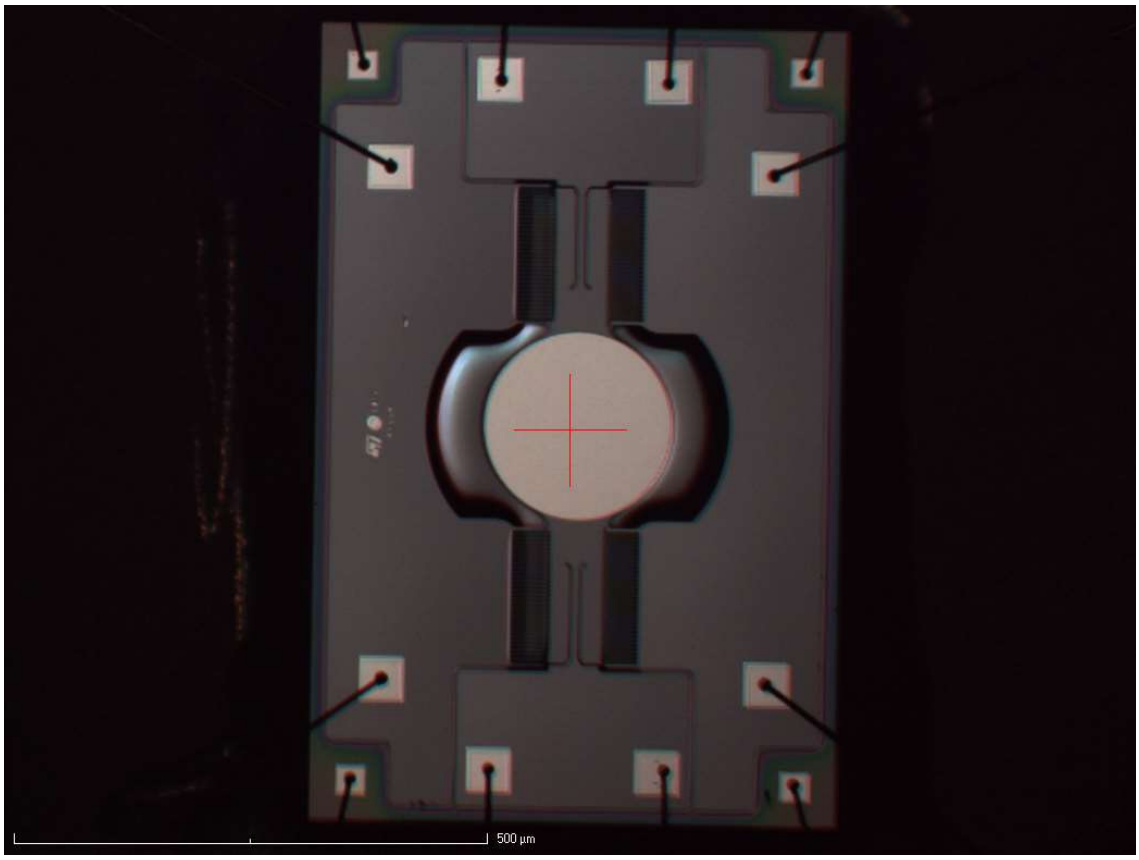

Figure 3-2: Microscope image of the micro-mirror used for testing

3.2.1 Energy transferred to the system

The maximum energy transferred into the system for a sinusoidal input and different oscillation amplitudes were calculated with a time domain simulation in MATLAB using equation (10).

$$E = \int_0^{t_{cycle}} \left(\frac{v^2 \frac{dC}{d\theta}}{2} \right) \frac{d\theta}{dt} dt \tag{10}$$

where t_{cycle} is the period, v is the instantaneous voltage, $\frac{dC}{d\theta}$ is the rate of change of capacitance with angle, and $\frac{d\theta}{dt}$ is the angular velocity. The rate of change of capacitance with angle was interpolated from data obtained from previously

performed finite element analysis of the micro-mirror [67]. This data is shown in Figure 3-3.

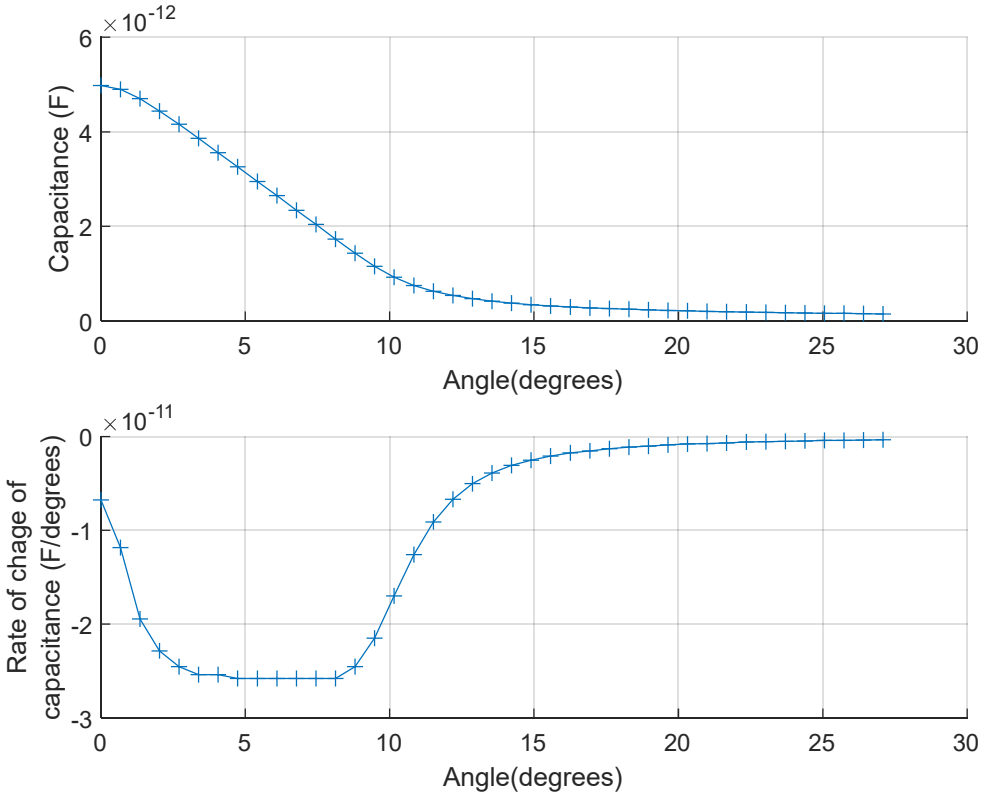

Figure 3-3: Capacitance and rate of change of capacitance against micro-mirror angle used in this study [67]

Figure 3-4(a) [68] shows that for a sinusoidal input of a constant amplitude of 200 V peak, the total input energy to the system increases with oscillation amplitude up to 20°, after which it starts to decrease. At micro-mirror angles above 20°, the comb structure is completely disengaged and the rate of change of capacitance with angle is nearly zero resulting in negligible instantaneous torque. As the amplitude of oscillations increases, a longer portion of the cycle occurs in the negligible torque section (above 20°), meaning that less energy is transferred into the system overall.

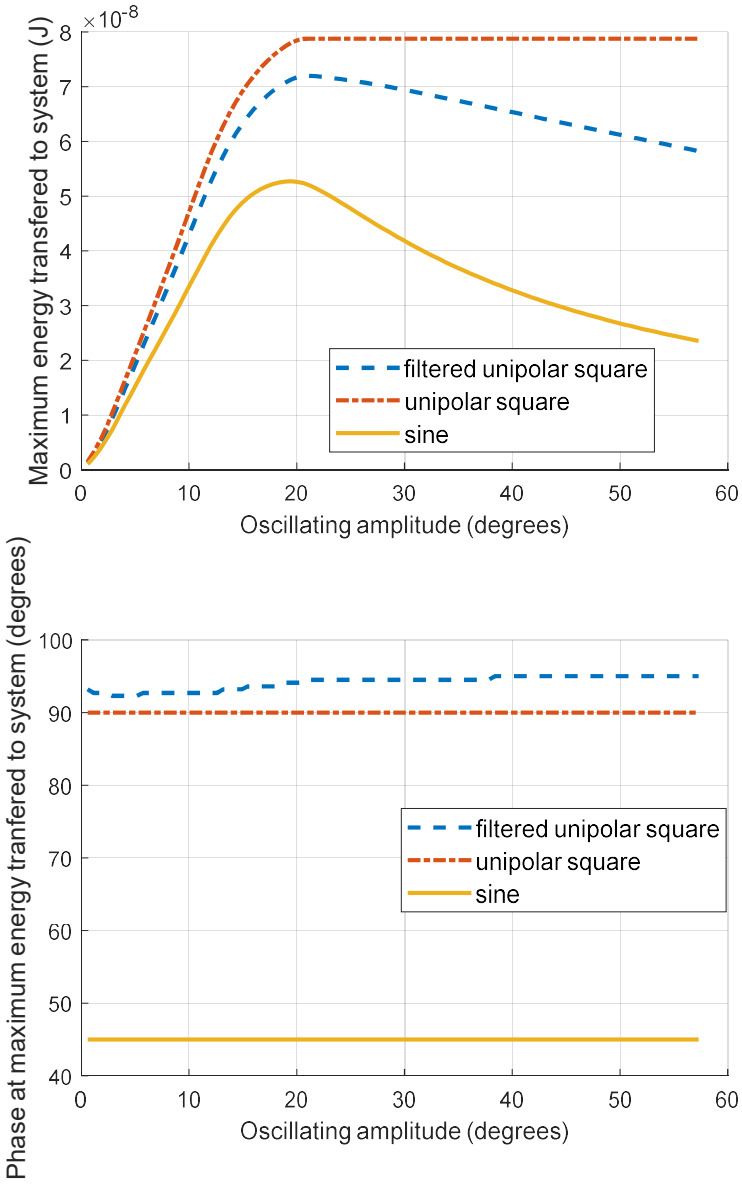

Figure 3-4:(a) theoretical maximum energy transfer to the system for different oscillating amplitudes; (b) theoretical phase between applied voltage and mirror angle at maximum energy transfer.

Since the micro-mirror is electrostatically driven and the force is related to the square of the applied voltage and not dependent on the polarity of the voltage, it can also be driven using a unipolar square wave with double the mechanical

resonant frequency. This results in the maximum possible energy transfer to the system since at optimum phase, the induced torque is always maximum when the dC/dθ is positive (mirror is returning to normal position) and zero when the dC/dθ is negative (mirror is moving away from normal position). The maximum energy transferred to the system for a square wave is also shown in Figure 3-4(a). Unlike the sinusoidal input, the total energy for the square input does not decrease as the oscillation of the micro-mirror increases. While negligible energy is transferred to the system when the comb structure is disengaged, a higher oscillation amplitude results in higher rate of change of capacitance at the start of the cycle, which results in the same energy input.

$$E = \frac{v^2}{2}\int_0^{\theta max} dC \tag{11}$$

The direct application of a high slew rate square voltage waveform results in a high current spike due to the input capacitance of the micro-mirror. These spikes in current can damage the mirror and the driver and can cause electromagnetic interference (EMI) to nearby circuitry. Moreover, micro-scanners are typically driven using high voltage of around 200 V peak, which in the event of a short failure, can result in dangerous arcing. This can be mitigated by introducing a resistor in series with the mirror. A typical resistance value is between 10 kΩ and 100 kΩ. This resistance together with the input capacitance of the mirror act as an RC filter to reduce the current spikes.

This means that the effective drive waveform is a filtered square wave. Figure 3-5 shows the three different waveforms considered to actuate the micro-mirror.

The resultant filtered square waveform which is used to drive the micro-mirror, together with a sinusoidal waveform and an ideal square wave, all with a phase of zero, are shown in Figure 3-5, and results in a decrease in energy transfer to

the system compared to the square wave. The waveform in Figure 3-5 was obtained from an experimental setup while driving the micro-mirror using a benchtop high voltage amplifier (Trek PZD350A) and a 100 kΩ current limiting resistor. The theoretical total energy transfer to the system for this waveform is also shown in Figure 3-4(a).

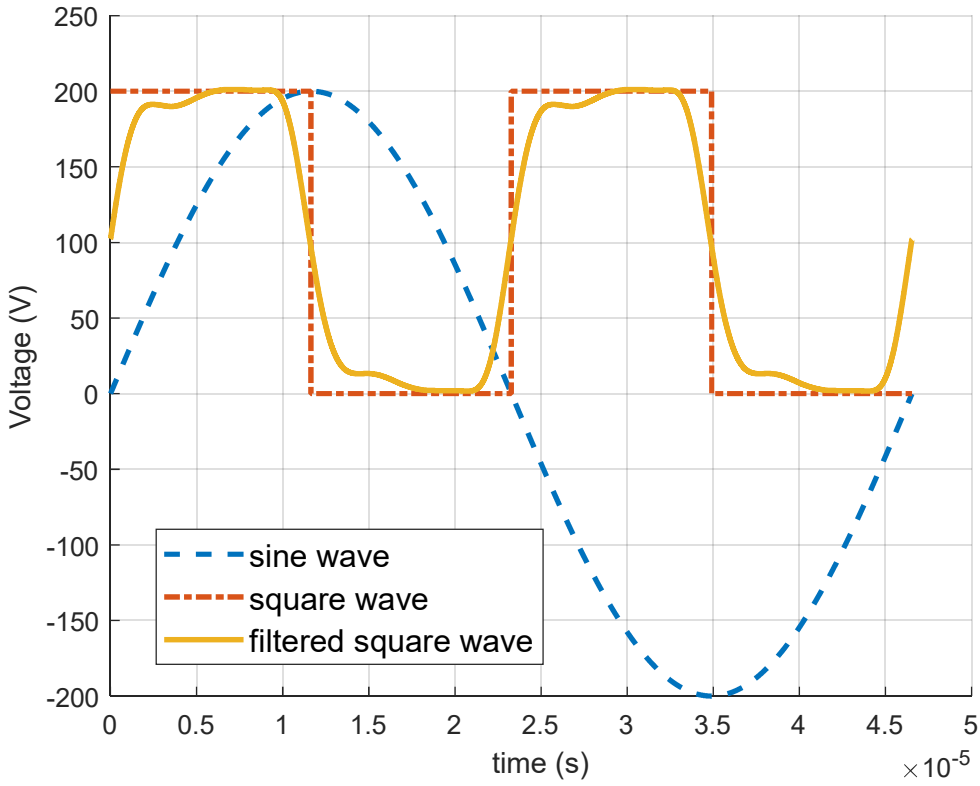

Figure 3-5: Different waveforms used to drive the micro-mirror (all displayed starting at zero phase)

3.2.2 Voltage – angular position phase at resonance

When operating resonant micro-mirrors, it is ideal that the mirrors are operated at their damped resonant frequency of oscillation. This results in the maximum achievable amplitude for a given maximum applied voltage constraint. This is usually obtained using a phased locked loop (PLL) which locks the phase in between the applied voltage and the output angle [30].

Under locked condition, the PLL achieves zero phase between the inputs of its phase detector, which in this case are the drive voltage and the mirror angular position. For this application, a specific phase adjustment is introduced to the drive voltage input path in order to ensure that the mirror operates at its damped resonant frequency. For this reason, it is important to determine the phase between the applied voltage and the mirror angle at the resonant frequency.

At resonance, the system exhibits the maximum energy transfer into the system. A MATLAB script was used to analytically evaluate the phase between input voltage and the maximum energy transfer to the system for different actuation waveforms. These theoretical results are shown in Figure 3-4(b). For a sinusoidal input, the optimal phase is found to be constant at 45°, while for a unipolar square wave, it is 90°. This indicates that under these conditions, operating the mirror using a PLL with the specified phase adjustment results in the maximum possible oscillation amplitude [68].

The phase relationship between applied voltage and angular position was also verified experimentally using the micro-mirror available. The results in Figure 3-6 show that for a sinusoidal input, the measured phase is constant at approximately 46° and for a square wave input the phase is constant at approximately 93°.

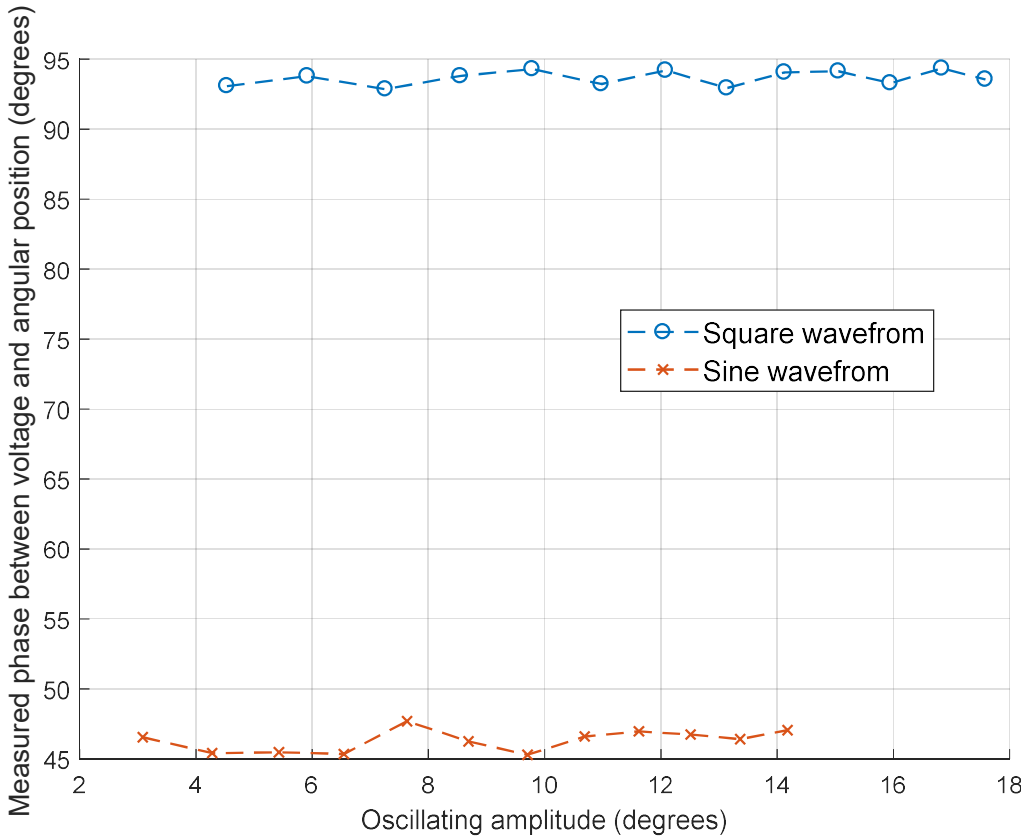

Figure 3-6: Measured phase between the applied voltage and angular position for sine and square actuation waveforms

The required optimal phase adjustment changes slightly when a filtered square wave is applied to the system. Further phase delays can be introduced in the angular position sensing mechanism. The proposed PLL-based controller used here incorporates an adjustable phase delay which can compensate for such inaccuracies.

3.3 Oscillation amplitude and phase measurement technique using a photodiode

The proposed technique uses the timing between pulses from a photodiode which is placed in the line of the laser path that is reflected off the micro-mirror

(Figure 3-7). A pulse is generated every time the reflected laser spot passes over the photodiode which is at a fixed position, and where X_1 and X_2 denote the limits of the photodiode width. In addition, X_1 represents the position corresponding to the rising edge of the pulse generated while the mirror is moving away from the neutral position and X_2 represents the position corresponding to the rising edge of the pulse while the mirror is moving towards the neutral position.

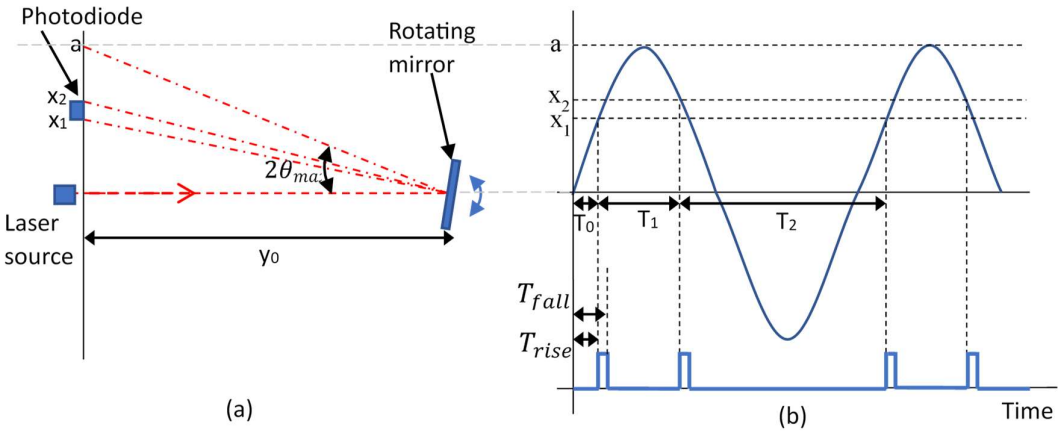

Figure 3-7: (a) Optical Setup (b) Corresponding projected laser spot position and photodiode signal waveform

The pulse width, T_p, produced by the photodiode is dependent on the frequency of the mirror oscillations, the amplitude of oscillations and the position of the detector. It can be determined using equation (12) where T_{rise} is the time from the beginning of the cycle to the first rising edge and T_{fall} is the time from the beginning of the cycle to the first rising edge. For the setup used, y_0 = 95 mm, x_1=1.8 mm, and x_2 = 5 mm which results in a minimum pulse length of 25 ns. The laser spot size determines the maximum pulse rise and fall time.

$$x_1 = \text{a } \sin(2\pi f T_{rise})$$

$$T_{rise} = \frac{1}{2\pi f}\sin^{-1}(\frac{x_1}{a})$$

$$x_2 = \text{a } \sin(2\pi f T_{fall})$$

$$T_{fall} = \frac{1}{2\pi f}\sin^{-1}(\frac{x_2}{a})$$

$$a = y_0 \tan(2\theta_{max})$$

$$T_p = T_{fall} - T_{rise}$$

Substituting in the above equation gives:

$$T_p = \frac{1}{2\pi f}\left[\sin^{-1}\left(\frac{x_2}{y_0 \tan(2\theta_{max})}\right) - \sin^{-1}\left(\frac{x_1}{y_0 \tan(2\theta_{max})}\right)\right] \quad (12)$$

A photodiode and an amplifier circuit shown in Figure 3-8 are used during all photodiode-based measurements. The circuit uses a APT2012PD1C photodiode to detect the laser beam as it passes over it. The diode is reverse biased to half the supply voltage and its current amplified using the LMV793 operational amplifier U1. The transimpedance gain of this first stage is set by resistor R_1 and is set to -10kV/A. Capacitor C_1 has been added for stability. The output is shifted up by half the supply voltage as shown in equation (13).

$$\mathrm{V}_1 = \frac{V_{DD}}{2} - I_D \mathrm{R}_1 \quad (13)$$

The second stage uses a difference amplifier to subtract the offset and further amplifies the signal. The gain of this stage is chosen so that the amplitude of signal V_2 is close to the supply voltage and set by the ratios R_2:R_3 and R_6:R_7, which are kept equal.

$$\mathrm{V}_2 = \frac{R_3}{R_2}\left(\frac{V_{DD}}{2} - \mathrm{V}_1\right) = \frac{R_3}{R_2} I_D \mathrm{R}_1 \quad (14)$$

The last stage is a ADCMP600 high speed comparator which compares the signal V_2 with $V_{DD}/2$ in order to convert the analogue signal to digital.

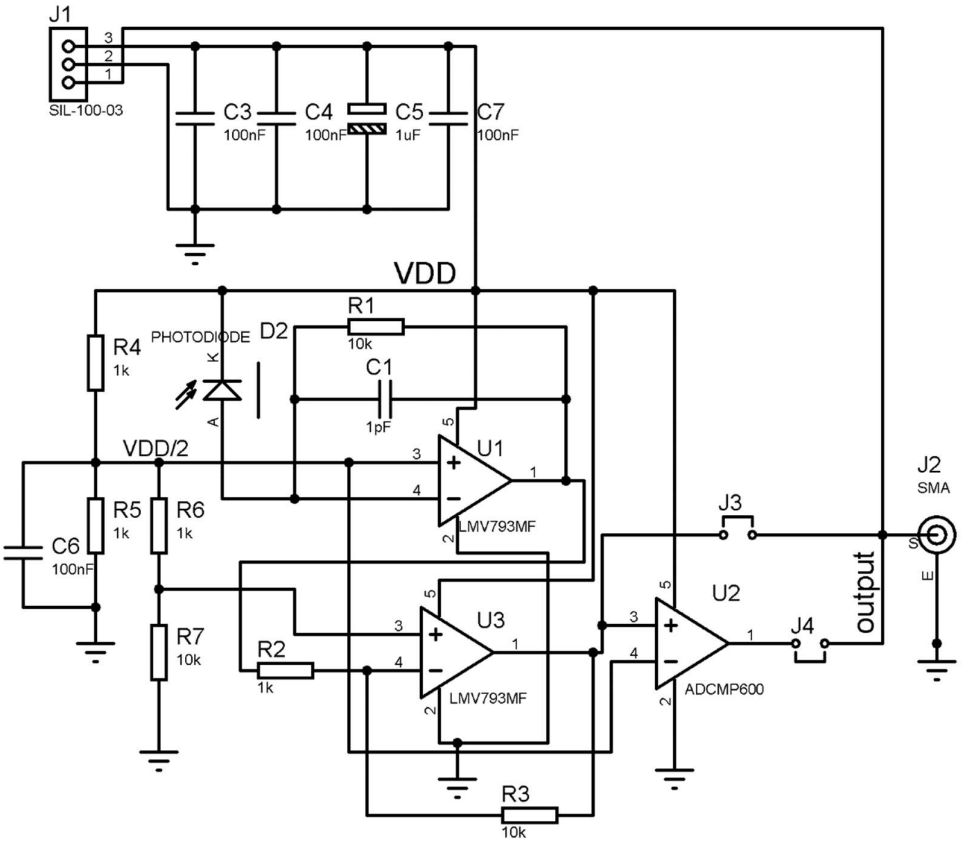

Figure 3-8: Photodiode detector circuit.

The simplest approach to finding the amplitude of oscillations is to use the centre of the photodiode pulse as a reference and then compute θ_{max} using (15).

$$x = a \sin(2\pi f(T_0))$$

$$a = y_0 \tan(2\theta_{max})$$

$$x = y_0 \tan(2\theta_{max}) \sin(2\pi f(T_0))$$

$$T_0 = \frac{T_2 - T_1}{4}$$

$$f = \frac{1}{T_2 + T_1}$$

$$\mathrm{x} = y_0 \tan(2\theta_{max}) \sin\left(\frac{\pi}{2}\left(\frac{T_2 - T_1}{T_2 + T_1}\right)\right)$$

$$\theta_{max} = \frac{1}{2}\tan^{-1}\left(\frac{\frac{x}{y_0}}{\sin\left(\frac{\pi}{2}\left(\frac{T_2 - T_1}{T_2 + T_1}\right)\right)}\right) \quad (15)$$

where x is the distance of the photodiode centre from the laser normal, y_0 is the distance of the photodiode from the mirror, and T_1 and T_2 represent the time measured between the photodiode pulses (Figure 3-7).

The inverse tangent in equation (15) results in the output being very sensitive to small errors in the timing measurement. One source of such error is the difference between the photodiode rise time and fall time, where the fall time is both slower and relatively inconsistent with variations in amplitude and environmental conditions. This has been demonstrated in published work, such as [48], where the authors could not obtain amplitude measurements using timing from a single photodiode and instead had to use two separate diodes in order to obtain the required results.

This difficulty is solved here by using only the rising edge of the photodiode pulse to determine θ_{max} [69]. The more consistent rising edge timing allows the use of a single photodiode. The use of only the rising edges of the pulses necessitates that the micro-mirror angle at the moment of the rising edge at X_1 (while the mirror is moving away from the neutral position) is not the same as the mirror angle at the moment of the rising edge at X_2 (while the mirror is moving towards the neutral position). T_0 can be calculated from T_1 and T_2 using (16):

$$x_1 = \mathrm{a}\sin(2\pi f T_0)$$

$$x_2 = \mathrm{a}\sin(2\pi f(T_0 + T_1))$$

$$\frac{x_2}{x_1} = \frac{\sin(2\pi f(T_0 + T_1))}{\sin(2\pi f T_0)}$$

$$\frac{x_2}{x_1} = \frac{\sin(2\pi f T_0)\ \cos(2\pi f T_1)}{\sin(2\pi f T_0)} + \frac{\sin(2\pi f T_1)\cos(2\pi f T_0)}{\sin(2\pi f T_0)}$$

$$\frac{x_2}{x_1} - \cos(2\pi f T_1) = \frac{\sin(2\pi f T_1)}{\tan(2\pi f T_0)}$$

$$\tan(2\pi f T_0) = \frac{\sin(2\pi f T_1)}{{x_2}/{x_1} - \cos(2\pi f T_1)}$$

$$T_0 = \frac{1}{2\pi f}\tan^{-1}\left(\frac{\sin(2\pi f T_1)}{{x_2}/{x_1} - \cos(2\pi f T_1)}\right) \tag{16}$$

where x_1 and x_2 are the distance of the photodiode edges from the normal axis, and T_1 is the shorter length between two pulses and f is the frequency of oscillations.

The maximum achievable angle, θ_{max}, can be calculated using (17). T_0 can also be used to calculate the zero-angle crossing time, from which the phase between the drive voltage and mirror angle can be estimated.

$$x_1 = \mathrm{a}\sin(2\pi f(T_0)$$

$$\mathrm{a} = \frac{x_1}{\sin(2\pi f(T_0)}$$

$$a = y_0 \tan(2\theta_{max})$$

$$\theta_{max} = \frac{1}{2}\tan^{-1}\left(\frac{a}{y_0}\right)$$

$$\theta_{max} = \frac{1}{2}\tan^{-1}\left(\frac{x_1}{y_0 \sin(2\pi f T_0)}\right) \tag{17}$$

The amplitude measurement technique was implemented on an FPGA. A block diagram of the measurement is shown in Figure 3-9. T_1 and T_2 are measured

using a running 25 MHz counter and fT_1 is then calculated by dividing T_1 by T_1 plus T_2. From fT_1 the lookup table address is calculated using equation (18). Two look up tables are used with their structure shown in Table 3-1. The lookup table returns 65536 (f T_1) for which the phase can be calculated. The second lookup table with the same address structure is used to obtain $1000\theta_{max}$.

$$addr = \frac{T_1 * 2048}{T_1 + T_0} - 512 \tag{18}$$

The look up tables are a very fast and efficient way to compute the non-linear equations (16) and (17).

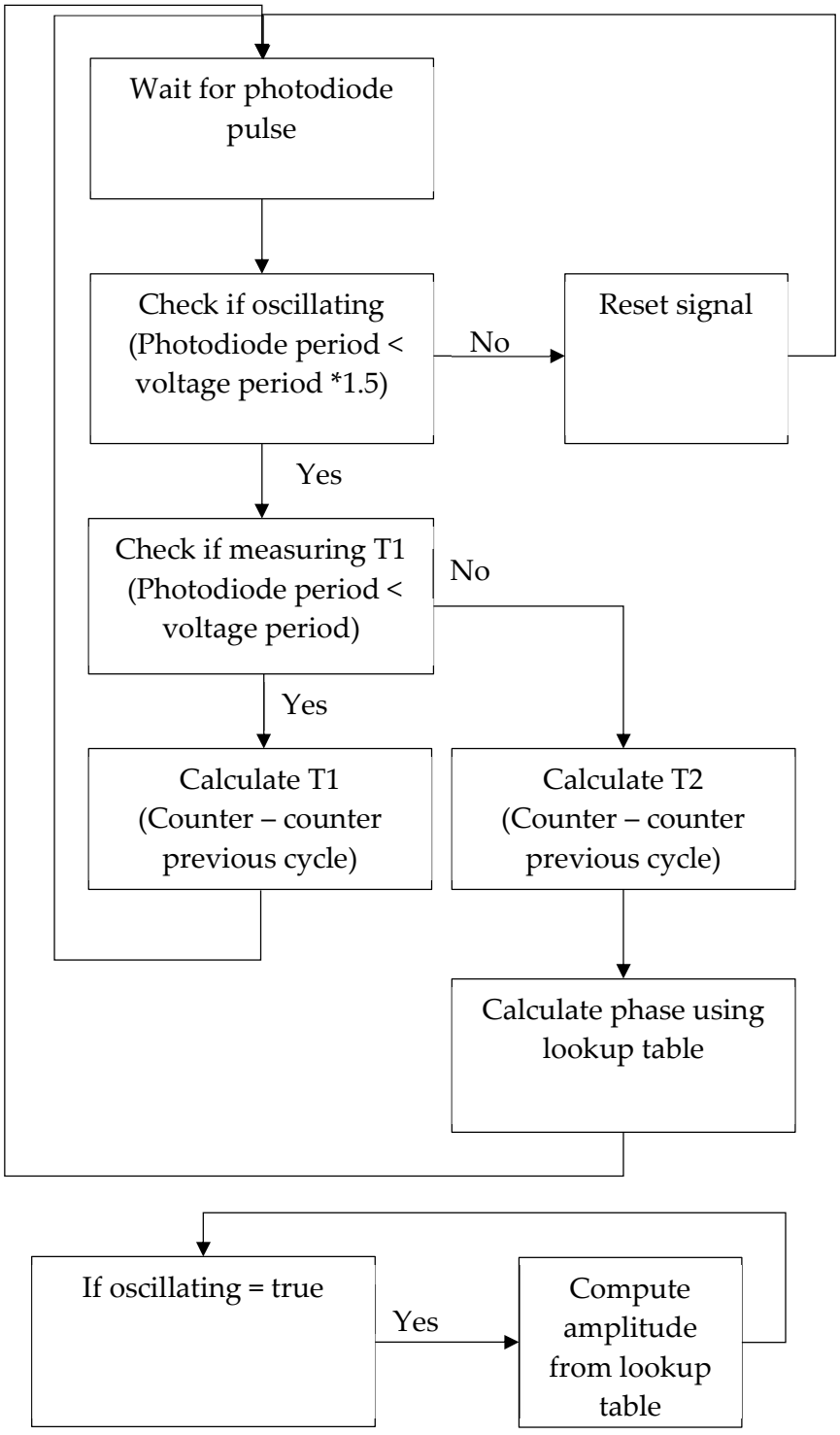

Figure 3-9: Phase and amplitude computation block diagram

Table 3-1: Look up table for amplitude and phase measurement

Address	X value (f*T1)	f T1	65536 (f T1)	Angle	1000 x Angle
0	0.25000	0.056330	3692	0.83964	840
1	0.25049	0.056271	3688	0.84048	840
2	0.25098	0.056212	3684	0.84132	841
3	0.25146	0.056152	3680	0.84218	842
4	0.25195	0.056092	3676	0.84304	843
5	0.25244	0.056032	3672	0.84391	844
6	0.25293	0.055971	3668	0.84478	845
…					
507	0.49756	0.000659	43	20.27589	20276
508	0.49805	0.000527	35	20.88309	20883
509	0.49854	0.000395	26	21.49879	21499
510	0.49902	0.000263	17	22.12103	22121
511	0.49951	0.000132	9	22.74771	22748

Figure 3-10 shows the frequency response of the micro-mirror obtained using the photodiode and PSD measurement methods, where a good agreement between the two techniques can be observed with a maximum difference in measurement of 4.8%.

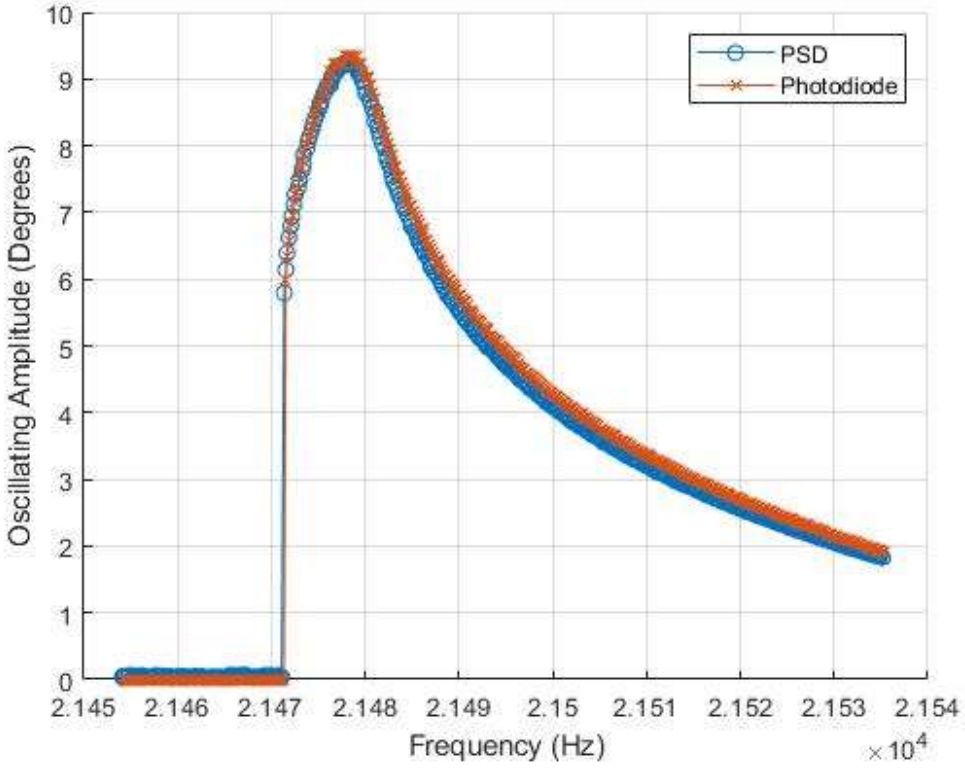

Figure 3-10: Measured oscillation amplitude of micro-mirror using PSD and photodiode pulses

3.4 All-digital implementations

As described in Section 3.1, the ideal waveform to actuate the AVC micro-mirror is using a unipolar square wave at double the resonant frequency, rather than a bipolar sinewave at its resonant frequency. The micro-mirror used has a resonant frequency of approximately 21 kHz and therefore should be driven by a 42 kHz square wave. This is typically achieved using an analogue system, where a voltage-controlled oscillator (VCO) is driven using a digital to analogue converter (DAC). In this study, the controller is implemented in all-digital logic and therefore avoided the use of a VCO and a DAC. The simplest way to generate the output waveform is to use a digital divider, where the system clock is divided by a counter having a value equal to the input clock

frequency divided by the output clock frequency. Assuming a digital system with a maximum operating frequency of 100 MHz, the frequency resolution using an integer divider is approximately 16 Hz. Since the bandwidth of the micro-mirror is approximately 20 Hz, with this resolution it is not possible to operate the mirror at its resonant point.

In order to improve the output frequency resolution, a fractional-N divider is used. The fractional N-divider, described in Section 2.3.2, is set up so that it switches between two adjacent integer dividers within a window of 11.9 ms, which is equal to half the output clock period multiplied by 1000. Equation (7) is used to calculate the ratio between the time window for "divide by N" and the time window for "(divide by N-1) + (divide by N)", as shown in Figure 3-11. This effectively increases the output frequency resolution by a factor of 1000 and an approximate resolution of 0.016 Hz is achieved, which is much smaller than the micro-mirror bandwidth

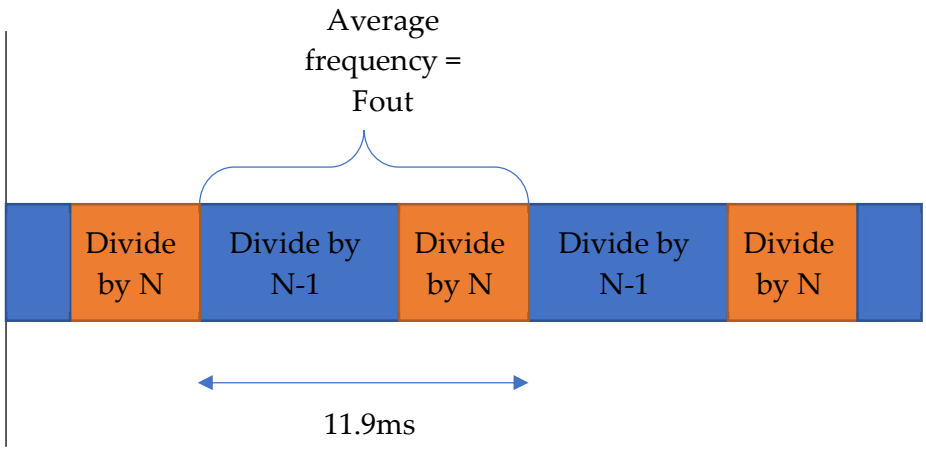

Figure 3-11: Integer divider timing

The fractional-N divider described above can be improved by randomizing the distribution of divide by N and divide by N-1. This is achieved using a delta-sigma fractional-N divider. The timing diagram is shown in Figure 3-12.

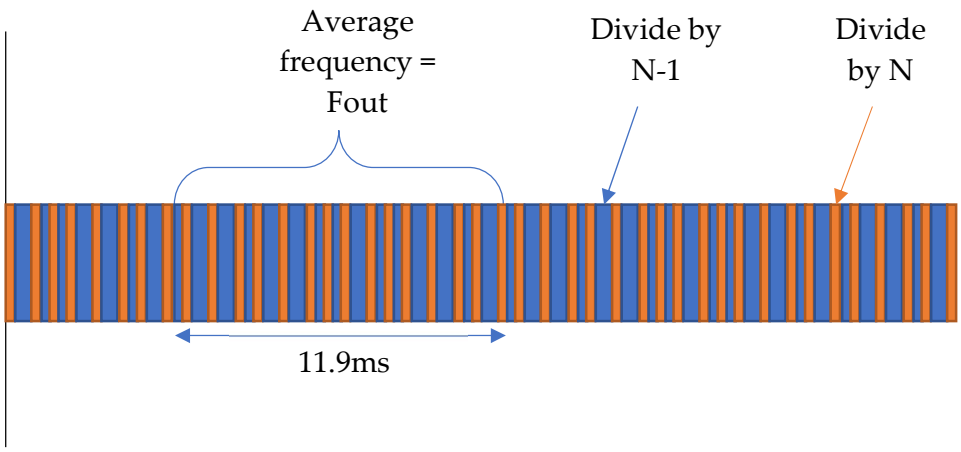

Figure 3-12: Delta sigma fractional-N divider timing

The single order delta-sigma fractional-N divider was also implemented on the FPGA. The delta-sigma modulator distributes the integer divisions randomly across the 12 ms window.

A dithering approach was also implemented on the FPGA. In this approach, the ratio between the two integer frequencies is always 1:N, where N changes so that the centre frequency is equal to the required frequency. This is achieved by counting in steps of 1000 until the total is larger than a target which is equal to the step size multiplied by the input frequency and divided by the output frequency. When the target is exceeded, the counter is not reset to zero. The target value is instead subtracted from the counter. This therefore means that at the start of the next cycle, the counter is loaded with the overflow from the previous cycle. The overflow keeps adding up over each cycle until it is larger than the step size and therefore results in the cycle requiring one less count to

exceed the target. A block diagram of the dithering approach is shown in Figure 3-13.

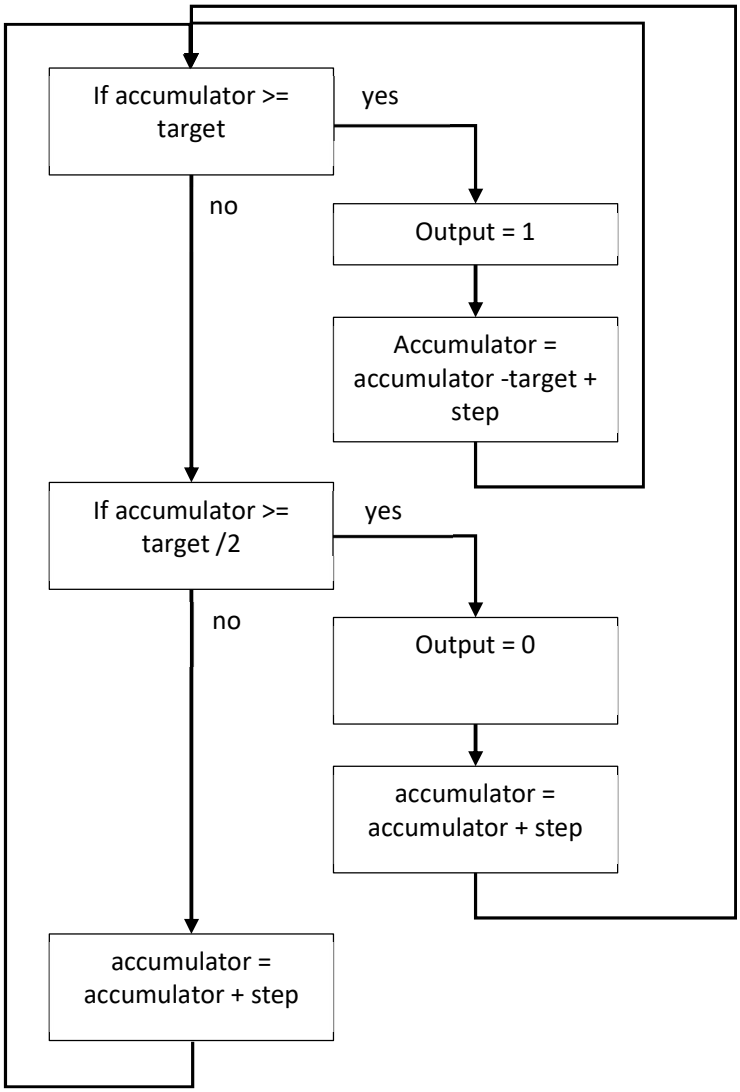

Figure 3-13: Block diagram for dithering approach implementation.

The resultant output frequency switches between the two integer divisions in a pseudo random pattern and has a similar effect to a delta-sigma fractional-N divider. The spurs in frequency response are pushed away from the centre frequency. Unlike the delta-sigma fractional-N divider, the dithering approach

does not repeat over a fixed time window but instead the sequence length is dependent on the output frequency.

The value of the target T is calculated using equation (8) with a step S of 1000 and F_{in} of 25 MHz and F_{out} chosen depending the resonant frequency of the micro-mirror.

$$T = \frac{S\,F_{in}}{F_{out}} \tag{19}$$

Testing of the all-digital resonating micro-mirror actuator was carried out on an angular vertical comb-drive micro-mirror with a diameter of 1 mm and resonant frequency of approximately 21 kHz.

The testing setup shown in Figure 3-14 has been used to accurately measure the mirror oscillation amplitude using the photodiode technique described in Section 3.3. Additional functionality was added to measure the maximum and minimum amplitude to the mirror during a one-second window. A delay of one-second was also added after changing the frequency in order to allow the mirror to settle to a steady state operation.

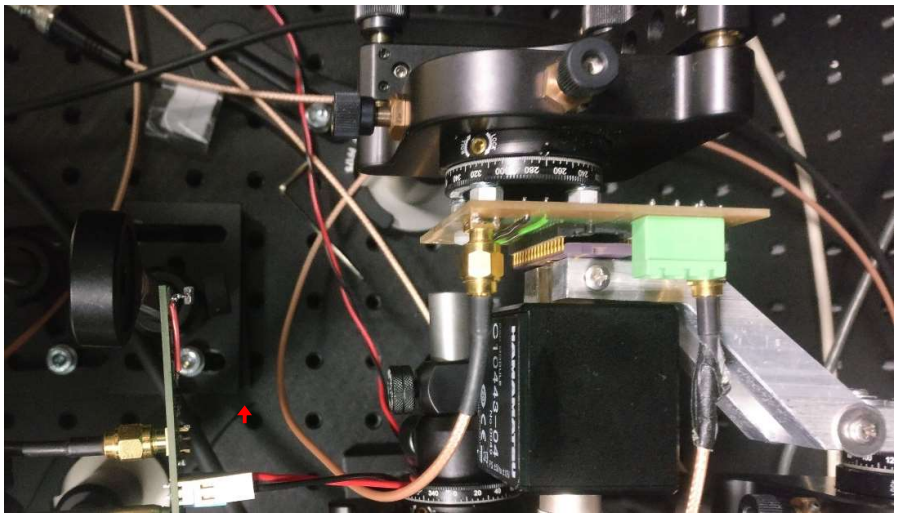

Figure 3-14: Optical setup using for measuring micro-mirror scanning amplitude

The all-digital driver was implemented on a Spartan 6 FPGA that was available at the University of Malta labs as a development board called Nexys 3. This FPGA model is reasonable priced as still offers 14570 logic cell, 2278 slices, 18224 flip-flops, a maximum distributed RAM of 136 Kb, and 232 user input/outputs [70]. The FPGA was operated at 25 MHz, which is a relatively low frequency that simplified the implementation on an ASIC later on in the project. The VHDL implementation for the three fractional-N dividers is shown in Appendix 1.

The maximum and minimum amplitude during a one-second window for a frequency sweep of a micro-mirror using the three techniques is shown in Figure 3-15. Figure 3-16 displays the amplitude range during the one-second window. The results show that a fractional-N divider results in an amplitude variation of the mirror response. This occurs since the spurs introduced by the fractional-N divider are within the bandwidth of the micro-mirror. Both the delta-sigma modulator and the dithering techniques shift the spurs away from the centre frequency. The shift of the spurs from the centre frequency can be seen in Figure 3-17. Both techniques perform equally better than the fractional-N divider when actuating the mirror in a stable manner. It is, however, noted that the dithering approach is simpler and more compact to implement.

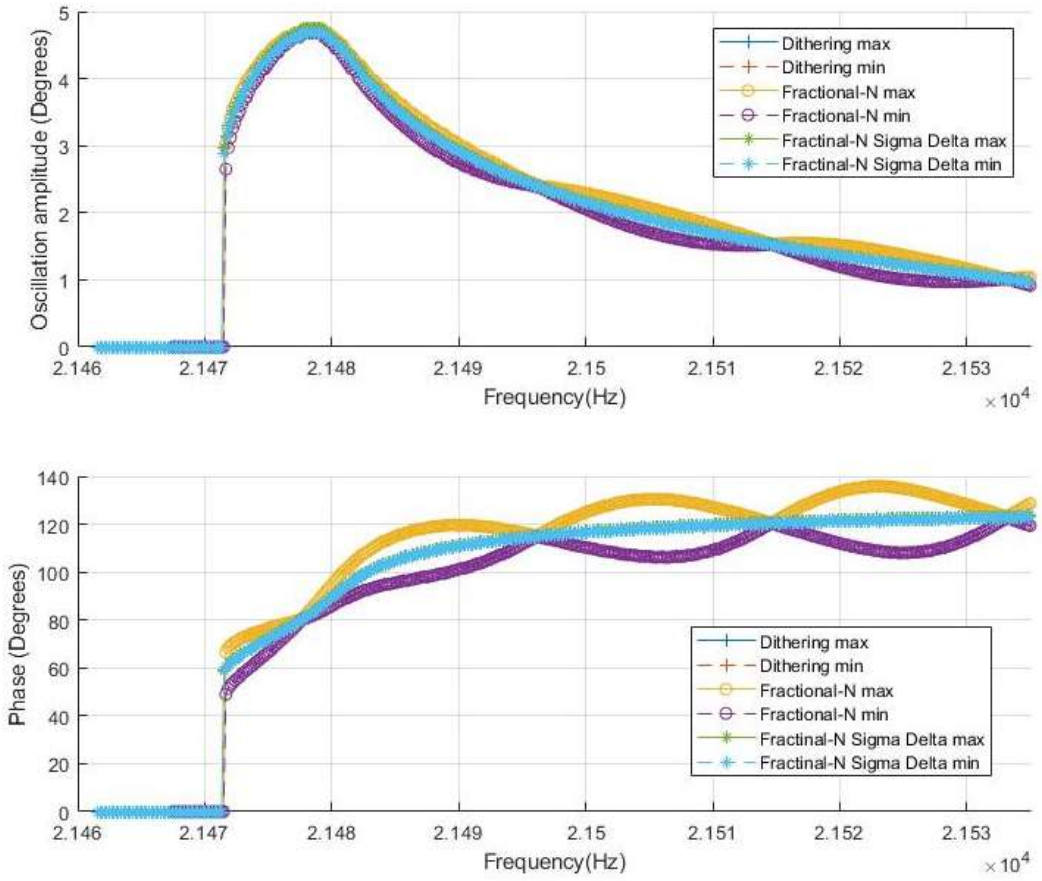

Figure 3-15: Maximum and minimum oscillation amplitude and phase using three types of fractional-N dividers

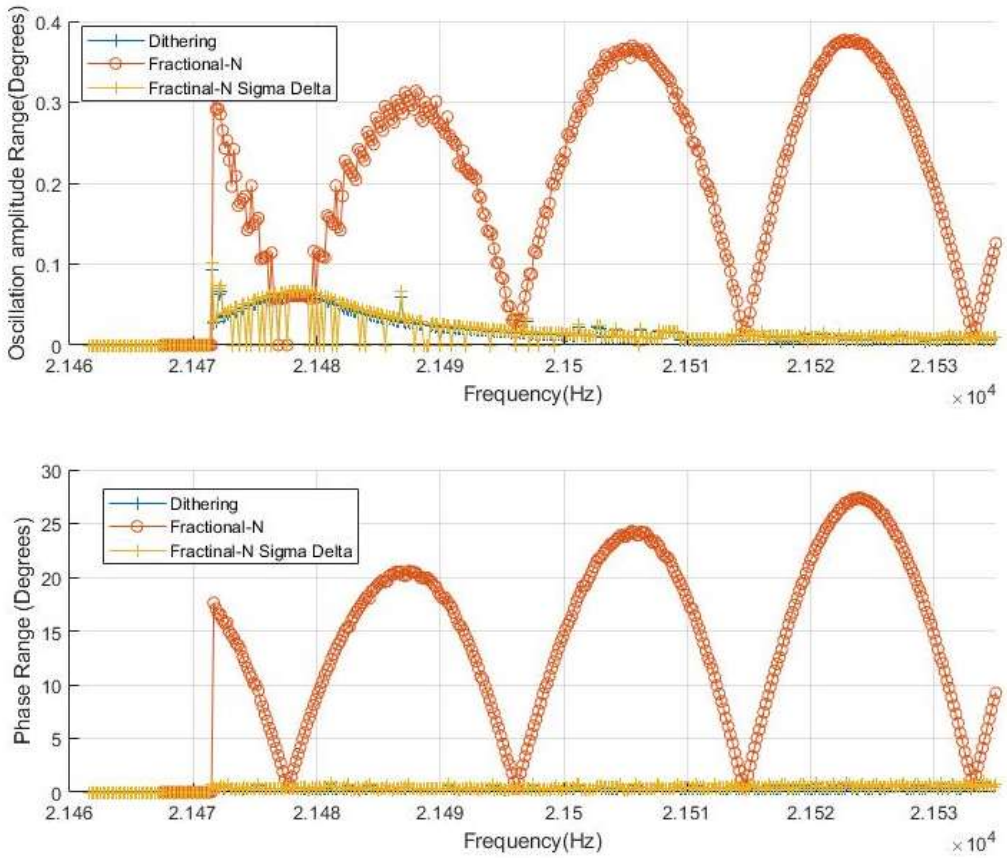

Figure 3-16: The difference between the maximum and minimum oscillating amplitude during a one-second window for the three types of fractional-N dividers implemented

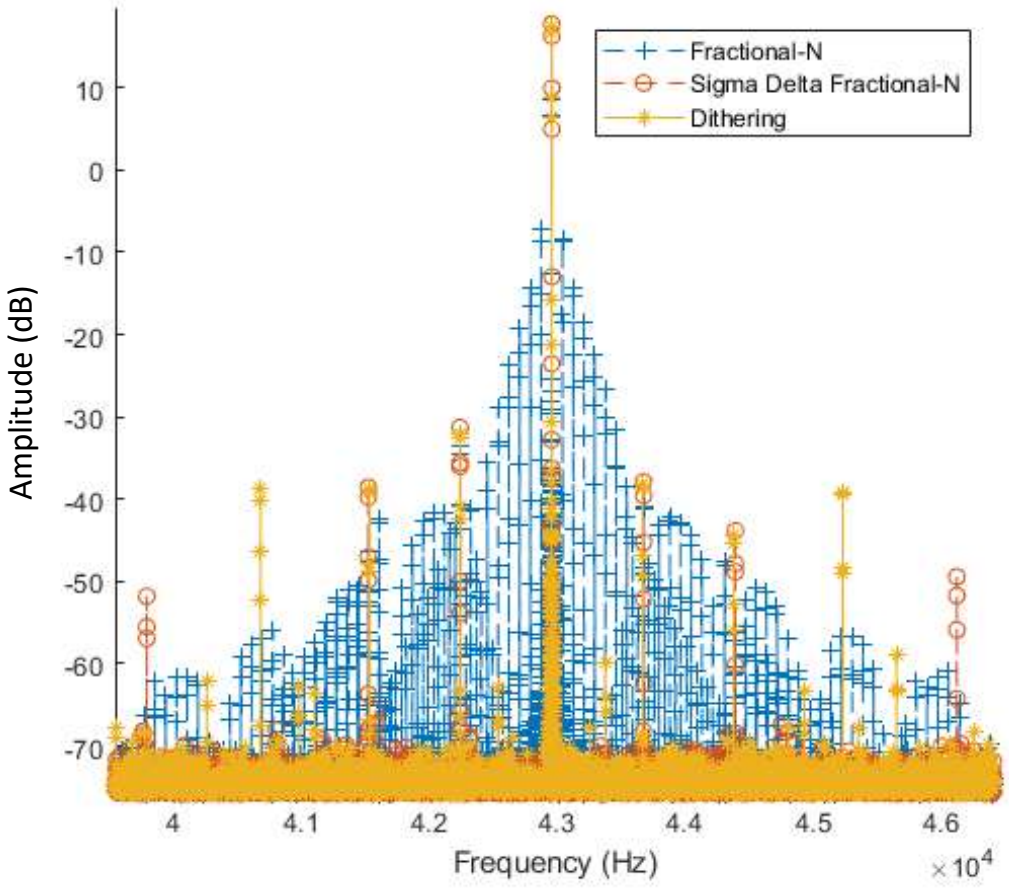

Figure 3-17: FFT response for Fractional-N divider, Delta Sigma Fractional-N Divider and Dithering divider. Values are normalized to a 20V reference and displayed in dB.

3.5 PLL and micro-mirror analytical model

Precise modelling of the micro-mirror is essential when designing an accurate controller for a micro-mirror. The PLL controller was simulated together with the micro-mirror using MATLAB Simulink. The micro-mirror model was simulated using a non-linear model which includes the electrostatic actuation as well as the mechanical second order model having non-linear damping. The electrostatic actuation was simulated using MATLAB and the model stored in a look up table, which was used to compute the rate of change of capacitance

of the micro-mirror. The model parameters were derived from Finite Element Modelling (FEM) simulations carried out on an actual mirror design.

In ideal conditions where the mirror is completely planar, there is no resultant force when a voltage is applied to the micro-mirror. In practice the armature of the mirror will not be exactly planar with the stator structure, resulting in a slight offset which introduces a small initial torque, essential for the start-up of oscillations. In simulation, this is modelled by applying an initial angular offset to the mirror at the start of simulations. The feedback technique considered in the model in Figure 3-18 consists of a photodiode in the optical path of the reflected laser beam. This photodiode produces two pulses per cycle which are used to calculate the time when the mirror is in its normal position. Using a counter, the time interval between the rising edge of the applied voltage and the mirror normal position is calculated. This time interval, which is proportional to the phase between the applied voltage and mirror angle, is then compared to threshold value normally set to one fourth the cycle time

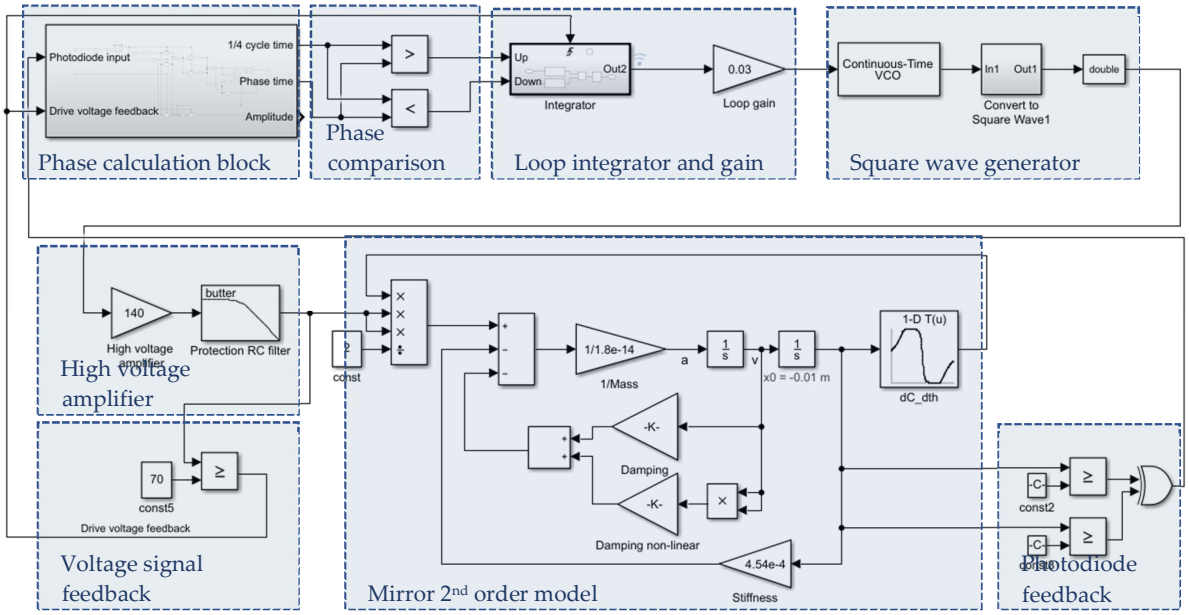

Figure 3-18: Simulink model for phase locked loop controller and micro-mirror

(equivalent to 90° phase). The threshold can be optimised to compensate for different actuation techniques and different mirror properties. The phase error is used to drive a loop integrator and gain which feed into the frequency adjustment input of square wave generator.

The simulation results presented in Figure 3-19 [68] show that the PLL can be used to actuate the mirror at its resonating point. The mirror oscillations increase up to a maximum stable amplitude of 10° when a 140 V peak square wave signal is applied. This stable oscillation amplitude is achieved in less than 120 ms. The phase between the driving signal and the output angle is 90°, which agrees with results obtained in Section 3.2. During the initial transient period, the output amplitude fluctuates slightly. This initial transient response is dependent on the initial conditions of the mirror.

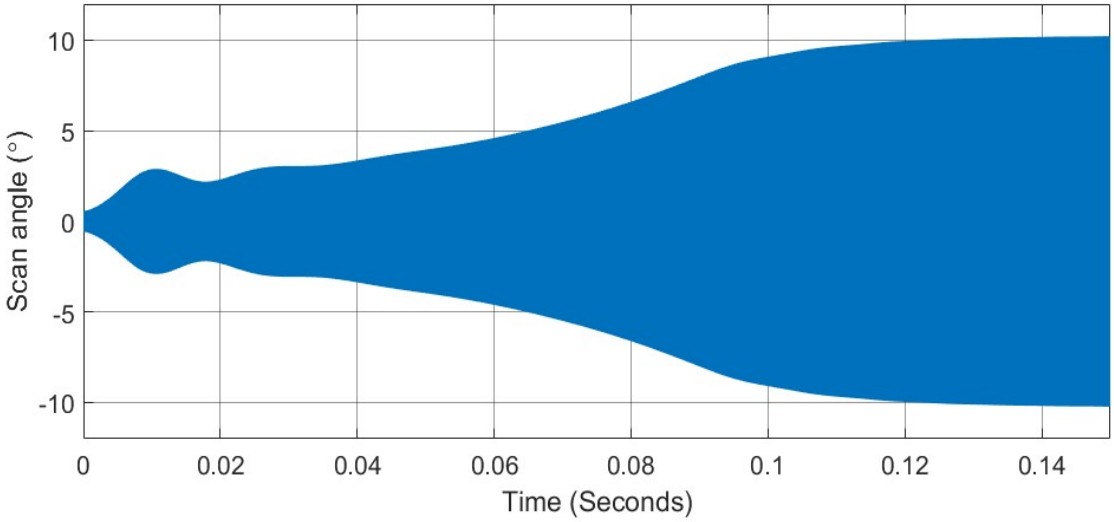

Figure 3-19: Simulation results for phase locked loop controller

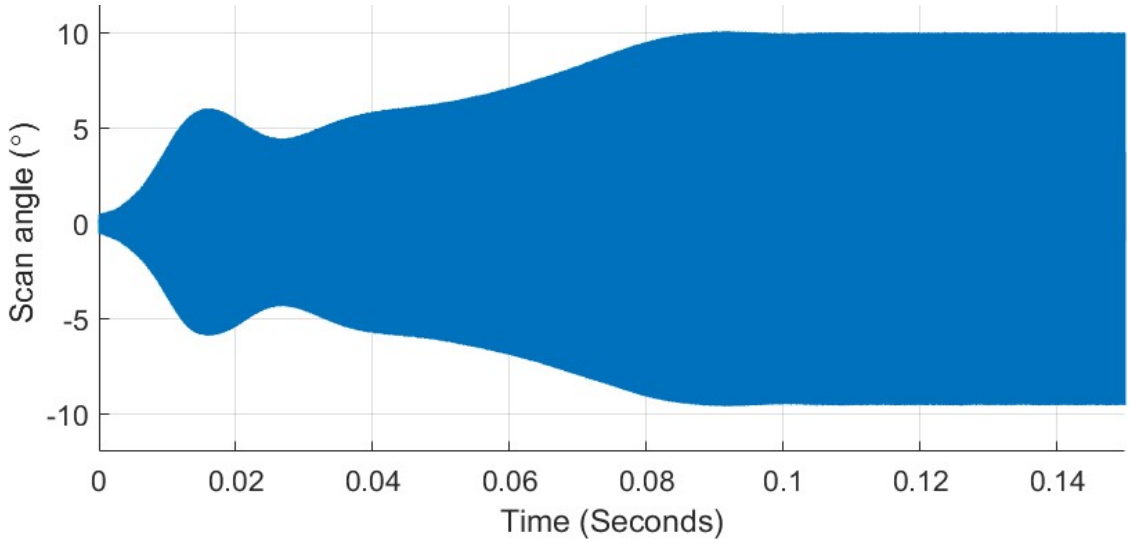

Figure 3-20: Measurement scan angle using all-digital PLL controller

This control system was implemented in digital circuitry using an FPGA. This was achieved using Xilinx ISE [71] software package. The overall design flow is shown in Figure 3-21. The first step was the development of the controller in VHDL. This was then synthesised and implemented using the Xilinx ISE built in tools. The bit file generated in the implementation is then programmed on the FPGA using the iMPACT programming tool [72]. The controller was then tested on the FPGA and its performance evaluated.

The inputs to the control system, which consist of the voltage drive feedback and the photodiode signal, are both digital signals. The output of the FPGA is a unipolar square wave and can therefore be used to drive the high voltage amplifier directly. The implemented feedback mechanism using a single photodiode cannot measure the amplitude and phase of oscillations when the amplitude is below a threshold. For this reason, a start-up procedure was implemented that sweeps the output frequency between two points until a stable input is achieved. When a stable input is achieved, the system switches from the start-up procedure to phase-locked loop control mode.

Experimental results were obtained on a micro-mirror using Position Sensitive Detector (PSD) for measuring the instantaneous angle. The resultant measured response is shown in Figure 3-20. A stable oscillation amplitude was achieved after an initial transient period of approximately 100 ms, which is comparable to that obtained using simulation.

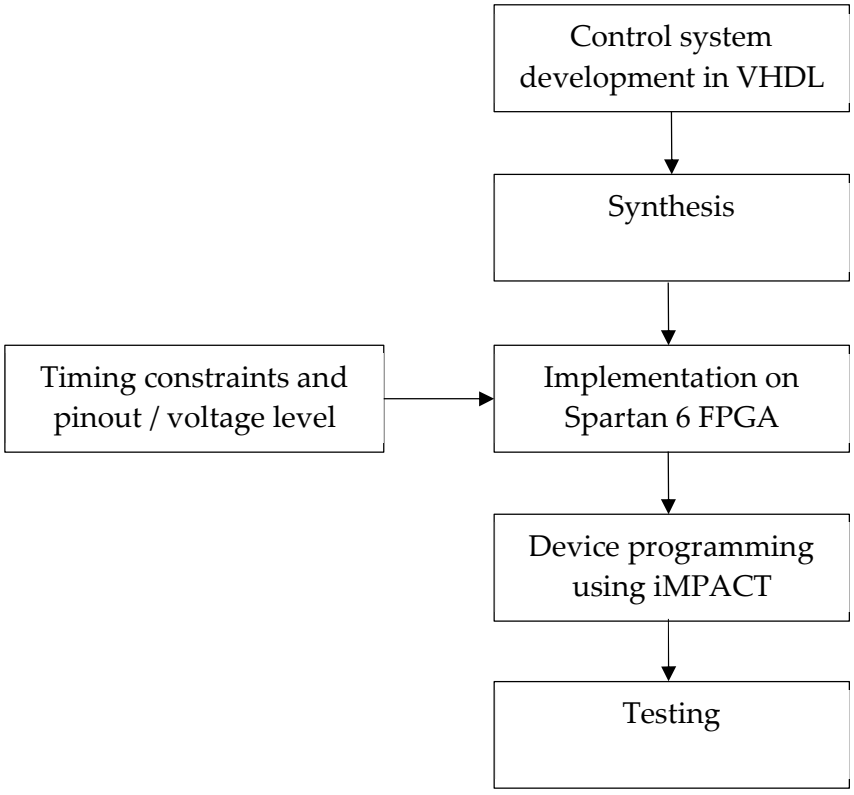

Figure 3-21: Development flow diagram for the controller implementation on the FPGA

3.6 Duty cycle amplitude control

Amplitude control is an important factor in micro-mirror devices. This is especially important in micro-spectrometers since any change in amplitude results in a shift in the spectral response. Open loop operation would not be possible since any variation in environmental conditions (such as temperature and humidity) will also affect the amplitude of oscillations.

There are three ways to adjust the amplitude of the micro-mirror – by varying the amplitude of the drive waveform; by varying the duty cycle of the waveform; and by changing the phase of the PLL controller.

In order to vary the amplitude of the drive waveform, a controllable power supply or an analogue amplifier is needed. These are more complex to implement when compared to the proposed all digital implementation.

Varying the phase of the PLL controller is also an option; however, the micro-mirror exhibits non-linear response with change in frequency as shown in Figure 3-10. This non-linear response has discontinuities with hysteresis between increasing and decreasing frequency sweep [73], therefore using phase to control the amplitude might result in a situation where the mirror turns off and a restart sequence would be required.

Duty cycle control is an effective way of varying the energy transfer to the system and is easy to implement in digital logic. The reduction in duty cycle can be obtained in two ways: by ending the pulse earlier and keeping the rising edge at 45° with the micro-mirror angle (waveform B in Figure 3-22), or by starting the pulse later and keeping the falling edge at 90° (waveform C in Figure 3-22). The non-linear nature of the micro-mirror actuation results in a different response in these two cases.

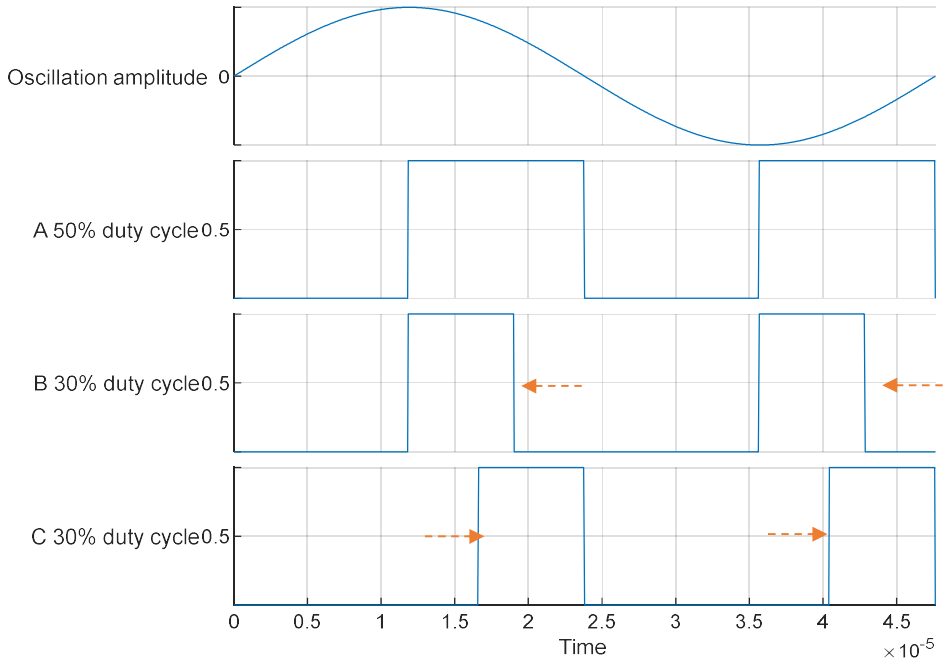

Figure 3-22: Comparing different techniques for change the duty cycle of the drive waveform

The implementation block diagram for the two approaches is shown in Figure 3-24 and Figure 3-23 and the code of the controller including the amplitude and phase control is shown in Appendix 2.

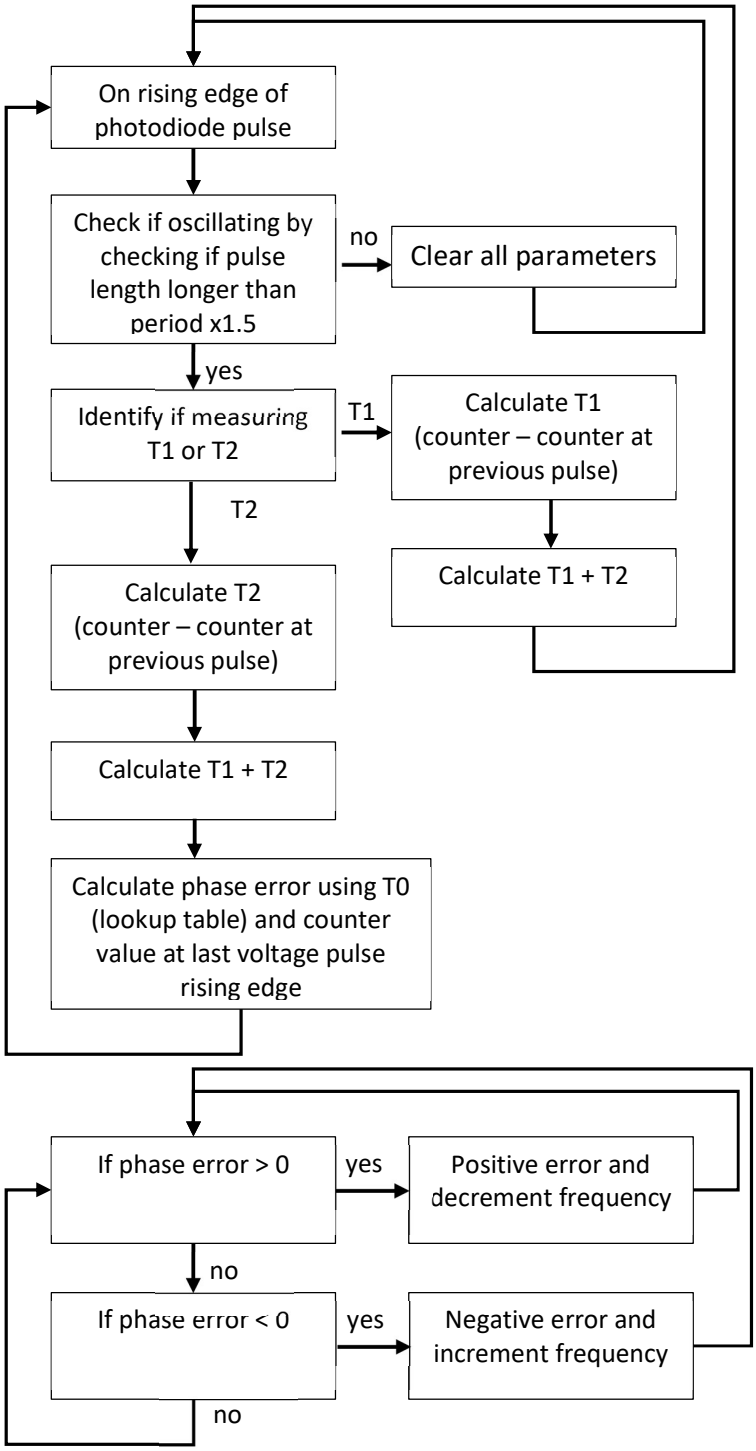

Figure 3-23: Block diagram for duty cycle control with leading edge fixed at 45°.

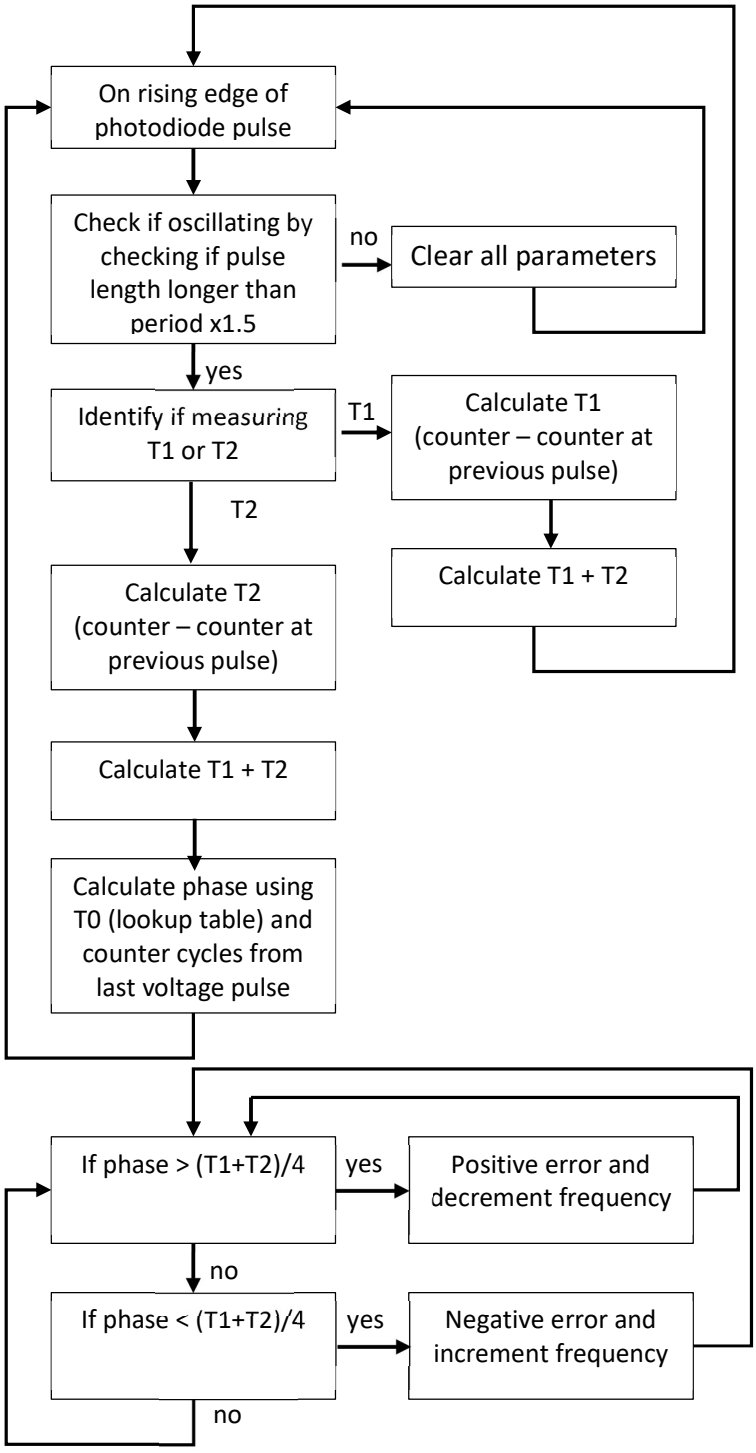

Figure 3-24: Block diagram for duty cycle control with trailing edge fixed at 90°.

The change in amplitude with change in duty cycle was found experimentally for the two cases and is shown in Figure 3-25 [74]. The second case where the falling edge is kept constant at 90° with respect to the mirror angle has a much more linear response with the applied duty cycle between 30% and 50%. Using this method allows for better response in the closed loop amplitude control since the system is more well behaved. This case also has a higher oscillation amplitude at a duty cycle of 55%. This is likely due to the fact that the applied waveform is a filtered square-wave and therefore the phase at resonance is slightly higher than 90°. Since with fixed rising edges the required linear response between duty cycle and oscillation amplitude was achieved, it was not necessary to investigate more complicated timing approaches.

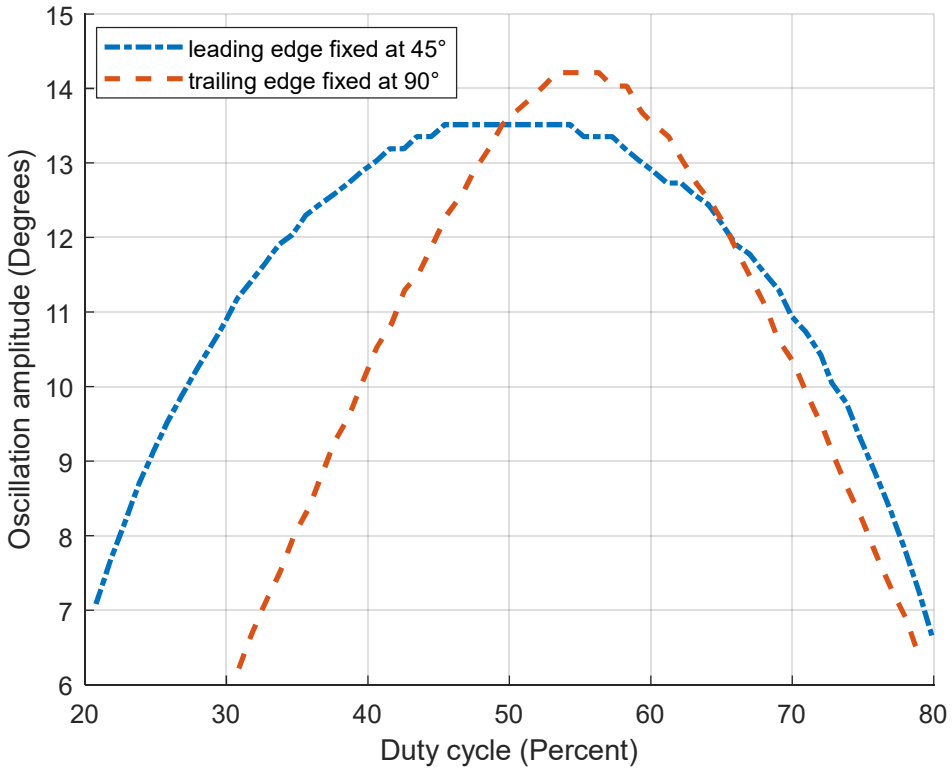

Figure 3-25: Comparing the measured change in amplitude with the two duty cycle approaches

3.7 Conclusion

A novel comparison between different waveforms that can be used to drive AVC micro-mirrors is first presented in this chapter. This comparison shows that for achieving maximum amplitude for a fixed maximum voltage in AVC resonating micro-mirrors, a unipolar square wave at double the mechanical resonating frequency is ideal. With a unipolar square wave, the maximum energy transfer is obtained for all angles. The higher energy transfer is significantly pronounced above the de-coupling angle of the comb drive. Above the de-coupling angle, sinusoidal drive at the mechanical resonant frequency loses its efficiency rapidly while square wave drive has no reduction in energy transferred at higher angles. For systems with low-pass filtered square wave drive (due to practical limitations in implementation) the performance is closer to the square wave drive than to sinusoidal drive. The ideal phase angle, for maximum energy transfer to the system, between the physical mirror angle and the drive signal was found to be 90° for square wave drive. The value of this angle is required in the synthesis of the appropriate drive signal when using a system such as a PLL. The ideal phase angle increases slightly for the case when a filtered square wave is used. These results present a clear distinction between the performance of different types of drive waveforms for electrostatic resonating micro-mirrors which can help micro-mirror controller designers make more informed decisions.

It is also shown analytically that it is possible to measure oscillation amplitude and phase at every cycle using only one feedback photodiode. This is achieved by relying only on the photodiode signal rising edge, which due to physical properties of the photodiode is more repeatable when taking into account environmental variations than the falling edge. Variations in the falling edge waveform effectively skew readings depending on the pulse midpoint. The analytical work is successfully validated using an FPGA implementation. The

proposed feedback mechanism is an improvement over previously published techniques [46] since both the amplitude and phase can be measured using a single photodiode. This is a novel solution to measuring the amplitude of oscillations of micro-mirrors and reduces the overall cost of the micro-spectrometer.

The work described in this chapter also shows that when varying the duty cycle for unipolar rectangular wave drive, the relationship between duty cycle and energy transfer is much more linear when the trailing-edge of the waveform is kept synchronised to the zero crossing of the mirror angular position. This is significant since a more linear response facilities the control of the amplitude even when the control parameters are not optimal. With this novel approach to duty cycle amplitude control of the micro-mirror oscillations, that is with synchronised trailing edge control, an integral controller was found to be sufficient, resulting in a simple digital implementation.

The combination of all the above results together was shown to be effective both with a numerical model, and with a physical implementation of a system comprising of a physical micro-mirror, a single-diode feedback system and square wave drive generated by a PLL.

Delta-sigma fractional-N division and dithering are both found to be effective solutions to the finite frequency resolution of the PLL. Both are superior to simple fractional-N division in terms of maintaining a stable mechanical oscillation frequency and amplitude. The advantage of the novel implementation of the dithering technique for synthesising the micro-mirror drive signal frequency versus the delta-sigma fractional-N method is that it requires less hardware to implement in a fully digital system.

4 ASIC Implementation

The testing carried out in Chapter 3 showed that the digital controller can be implemented on an FPGA; however, FPGAs are ideal when striving for the fastest time to market or if the hardware is planned to be reprogrammed to perform a different function in the future. An ASIC is a better option when the functionality is fixed and unchanging, while power consumption and lower unit cost are more important. An ASIC typically consumes less power when compared to the same logic on an FPGA [75]. Moreover, the same FPGA logic can be implemented in a much smaller die area. A typical area ratio of an FPGA to that of an ASIC is 21:1 [76].

As part of this study, the all-digital controller with its ancillaries has been implemented on an ASIC to demonstrate the feasibility of implementation for commercialisation purposes. A block diagram of a micro-mirror and the proposed closed loop controller is shown in Figure 4-1.

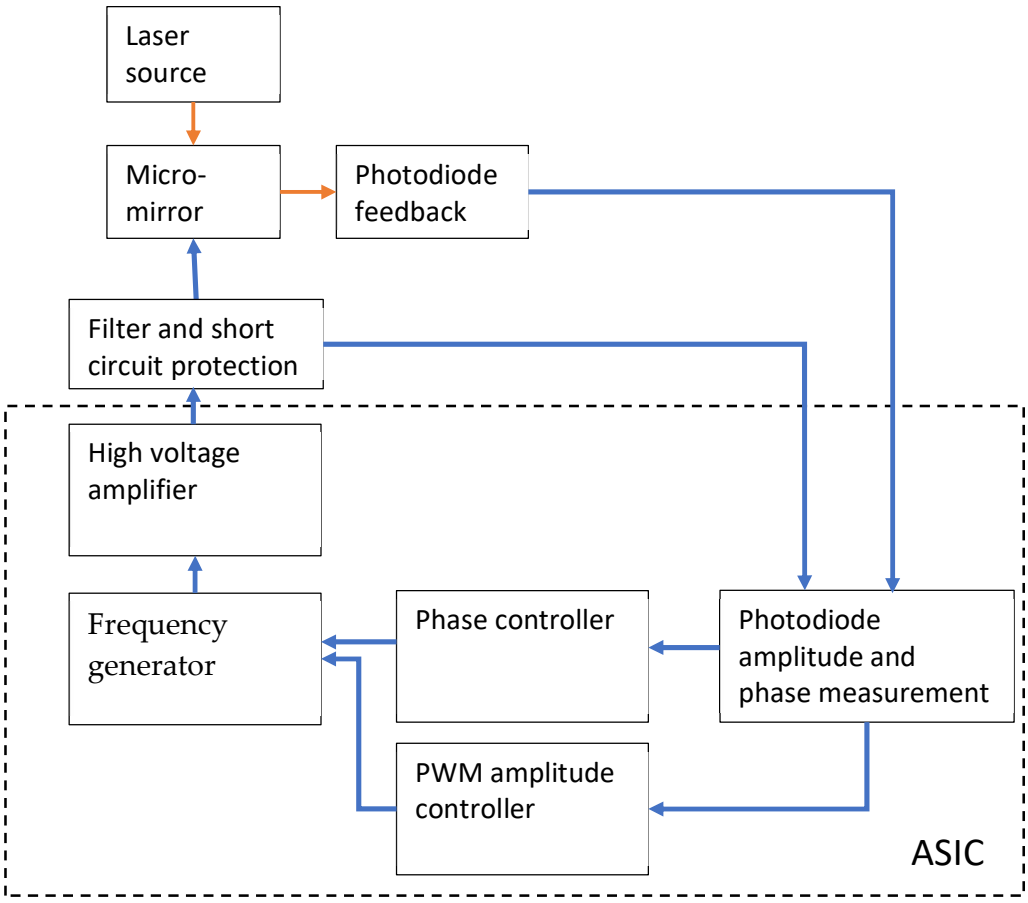

Figure 4-1: Block diagram of micro-mirror setup and proposed micro-mirror controller

4.1 Choice of implementation technology

The choice of technology for implementing the ASIC was limited to the MPW (multi-Project Wafer) runs offered by Europractice platform, which the University of Malta is a member of. Through such platforms, academic members are given access to various technologies by sharing wafer area and therefore distributing part of the manufacturing cost.

The proposed ASIC consists of two main sections: a high-density digital controller, and a high voltage analogue driver for the micro-mirror. The available micro-mirror requires a driving voltage of 200V. This means that to implement both the controller and the micro-mirror driver on a single die, a

technology with both low voltage digital and high voltage (up to 200V) analogue is required.

The only technology available within the Europractice platform that matches the requirement for this project at the time of manufacturing was the X-FAB XT018. This is a Bipolar-CMOS-DMOS (BCD) on Silicon on Insulator (SOI) process that combines low voltage digital and high voltage CMOS on the same die. A list of key process specifications is shown in Table 4-1.

Table 4-1: X-FAB XT018 process properties [65]

XFAB Xt018	
Wafer	8-inch p-type SOI
Minimum feature size	0.18μm
Digital voltage levels	1.8V, 5V
Metal layers	5 Al layers + thick metal layer
Max high voltage module	200V
Deep trench isolation	
Max operating temperature	175 °C
Density	125K gates per mm^2
Number of metal layers	6

The full title of the process used is X-FAB XT018 0.18μ SOI CMOS MET3/4/MID/THK. This process includes a total of 6 metal layers, the topmost being thicker than the remaining layers. The topmost layer can be used for power distribution in the IC.

4.2 Mixed mode ASIC Implementation

The controller implementation is divided into five silicon modules listed below. Figure 4-2 shows a block diagram of the five modules as implemented on the ASIC. The advantage of implementing the controller in separate modules rather than a single block, is that it ensures that if one module does not work, prototype testing could still be carried out on the remaining parts.

The five silicon modules shown in Figure 4-2, numbered 1 to 5, are as follows:

1. The complete digital logic together with a serial interface for updating lookup tables and parameters;
2. Amplitude and phase measuring logic;
3. Drive signal synthesis;
4. Debounce logic for conditioning the photodiode and voltage feedback signals;
5. Analogue high voltage driver.

Modules 2 and 3 are a replication of modules 1 without a debugging interface and lookup tables. This means that these modules are a better representation of a commercial micro-mirror controller and can be used to approximate the die area needed by the controller. Moreover, since the controller is implemented in two modules, the individually functionality of each can be tested.

The completed digital logic controller is implemented in an area of 1850 μm by 2350 μm. This controller includes a serial interface that is used to program the various features of the controller. A drawback of implementing modules 1 only is that if there are any problems with the serial interface the lookup tables cannot be loaded into the controller and thus it would not be usable. This means that the serial interface is a single point of failure to the overall operation of the full controller. For this reason, the controller is re-implemented in modules 2 and 3, shown in Figure 4-2, without any programmable memory. In this case,

the feedback measurement and the frequency generator are divided in two separate blocks which can be used together or individually, and parallel

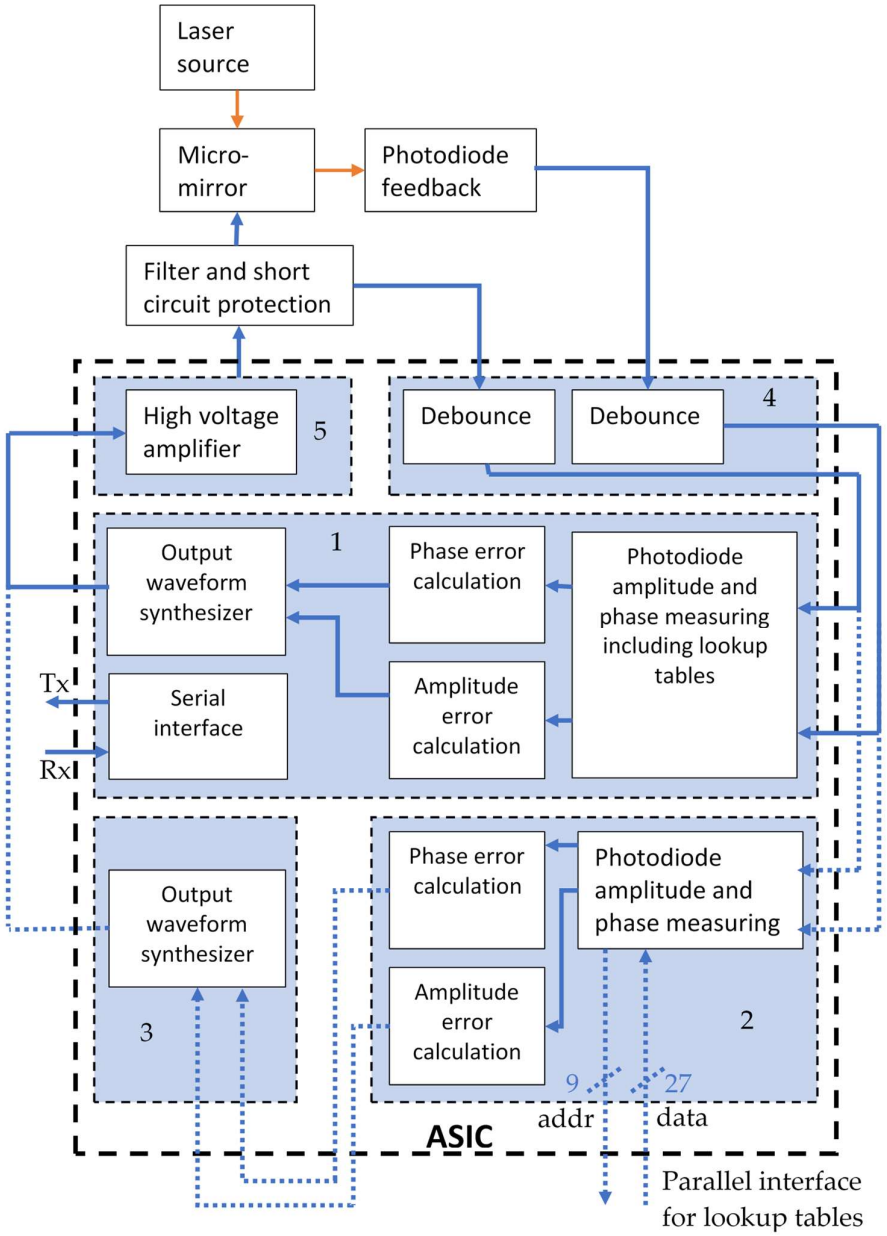

Figure 4-2: Detailed block diagram of the ASIC showing complete controller including the replicated modules (2, 3) implemented for testing purposes

interface is implemented to use lookup tables implemented externally (for example on an FPGA or a parallel flash IC). The look up table interface chosen is a simple parallel bus with 9 address lines and 27 data lines.

More details on the serial interface are presented in Section 4.2.2.1.

4.2.1 Main stages of physical layout

The overall process flow diagram is shown in Figure 4-3. The first step was to import the digital VHDL code of the control system verified on the FPGA into Genus synthesis tool [77]. The generated gate level netlist was then imported into Cadence Innovus [78] implementation system which includes placement, routing and timing optimisation of the physical layout. This is explained in detail in Section 4.2.2.

The analogue high voltage driver was designed and simulated using Cadence Virtuoso Studio. The Cadence Virtuoso layout suite [79] was then used to carry out manual implementation of the physical layout.

The digital and analogue physical layout were combined using Cadence Virtuoso layout tools and subsequently verified using Assura Physical Verification LVS [80]. The bonding pads and final routing for the complete ASIC were then placed, before exporting the final chip layout in .gds format. The die prototypes were fabricated at XFAB. The bonded prototypes were then characterised as described in Chapter 5.

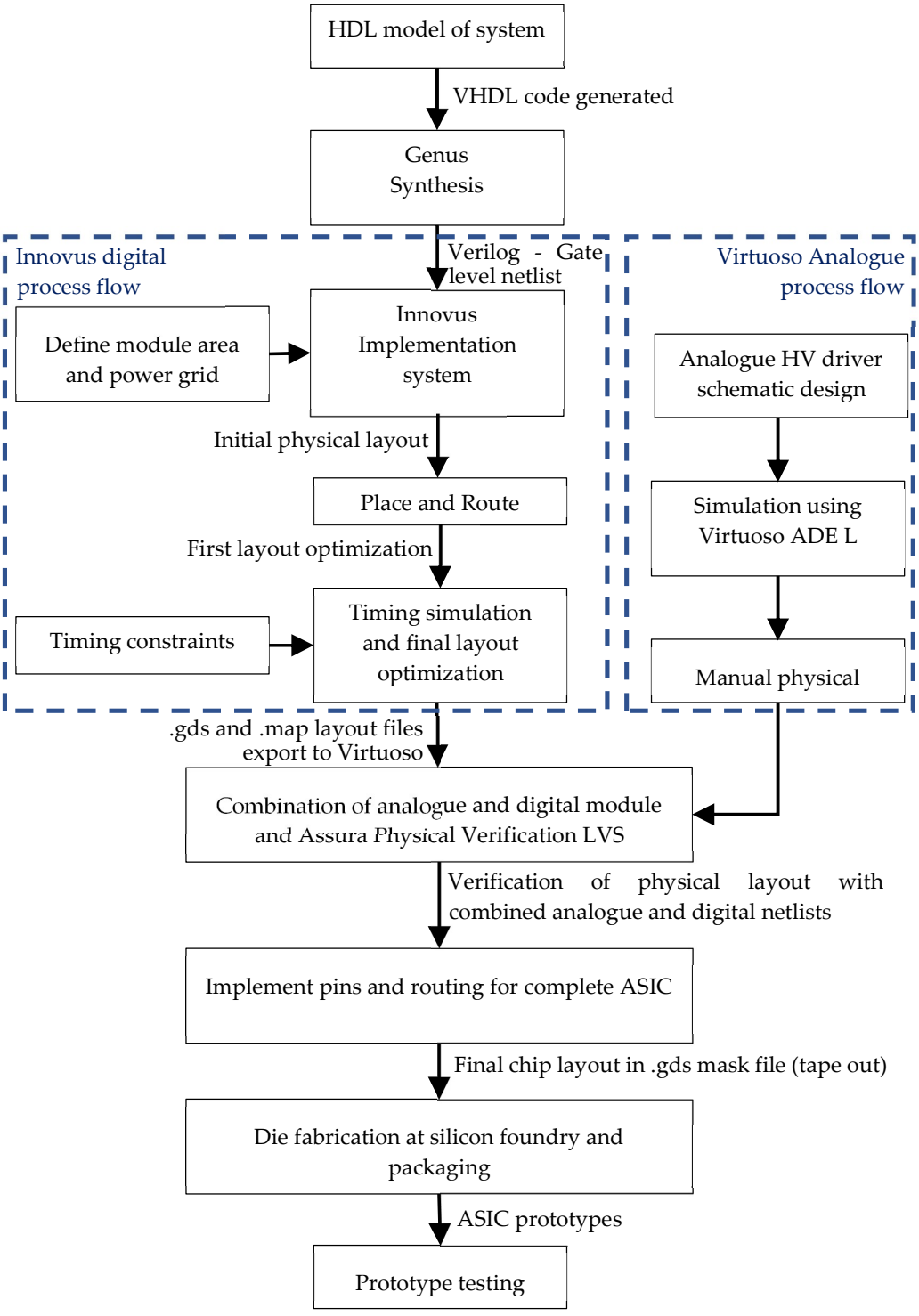

Figure 4-3: Design flow of the complete mixed mode ASIC

4.2.2 Implementation process for digital modules

Due to limitations in VHDL that do not allow for easy low level netlist generation, the VHDL files used in the FPGA implementation are synthesised and converted to a Verilog netlist using the Genus software package. This is repeated for all modules of the implementation.

The first step in implementation is to synthesise VHDL code into a gate level netlist which can be interpreted by Innovus software to create the layout. The gate level netlist is a low-level circuit description which contains only primitive instantiations and connectivity information. Verilog, being a lower-level language compared to VHDL, is more suited to describe the gate level netlist and is the only language that is accepted by Innovus as input. The VHDL code for every module 1 to 4 in Figure 4-2 is converted to Verilog gate level netlist using Genus software package [77]. The Verilog files are imported to Innovus [78] where all the input and output points are identified and an initial layout area is defined. Place and route tools are used to implement the layout followed by layout optimisation. Finally, each individual digital segment is imported to Cadence Virtuoso and combined to the necessary interface pads. Layout versus Schematic (LVS) is used to verify that the implementation is successful. During this process various design rule check tools were used to detect errors and correct them iteratively before arriving at the final layout to be used for manufacturing the design. The design process is shown in Figure 4-4.

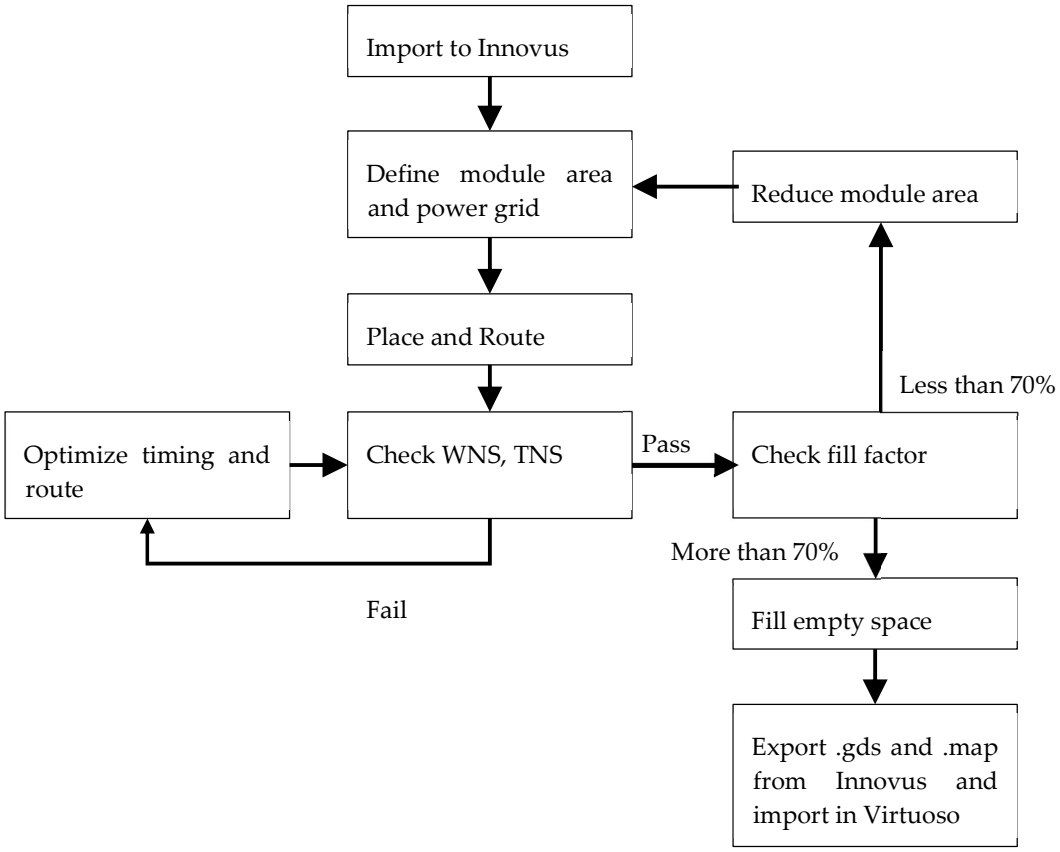

Figure 4-4: Detailed Innovus process flow for the digital modules

Genus is a synthesis tool that is used to generate a gate level netlist from the Register-Transfer Level (RTL) code of the project. As its input it uses the design VHDL code and XFAB libraries containing all the available cells for the chosen technology. The output consists of Verilog files containing the netlist equivalent of the VHDL code. The netlist uses only components from the Xfab D_CELLS_HD_LPMOS_typ_1_80V_25C library as these can later be implemented on the ASIC using the selected process. At this point a check was carried out to find pins connected to 'gnd' and update them to 'GND'. This has to be done since in the following steps, the Virtuoso package does not consider 'gnd' and 'GND' as part of the same net. Without this step the design would have two separate ground networks, causing an LVS failure.

The netlists were imported to Innovus and each module pinout, target area, VDD, and GND were defined. Two power rings, one for VDD and one for GND with vertical power stripes and horizontal power rows were added to ensure power distribution throughout the module. The cells in the netlists were placed in between the rows using the auto place tool.

Timing analysis was carried out to check the worst negative slack (WNS), the total negative slack (TNS), design rule violations (DRVs), and density of the circuit. If the WNS or TNS were negative or there were any DRVs a pre-clock tree synthesis (CTS) optimization was carried out to correct them. If the density was low, typically below 70% fill, the area was reduced by restarting the above procedure with a smaller defined area. If positive WNS and TNS could not be achieved the area was instead increased. Once all the criteria were met, CTS and Post-CTS optimisation were carried out while always verifying that WNS and TNS were positive. Routing was carried out followed by 'postRoute' timing analysis and post-routing optimisation. The last step was a geometry verification, and if no violations were present, the design was complete.

During cell placement some empty gaps are always left in between the power rows. These gaps would trigger a Design rule checker (DRC) error and were therefore filled with filler cells using the 'place cell' tool. The DRC also checks for the minimum metal rule and therefore dummy metal, connected to GND, was added to all layers using the 'add dummy metal' tool.

These modules were exported from Innovus as .gds and .map files and imported in Cadence Virtuoso to integrate the block in the final die layout. The netlists in the Verilog files were also imported to allow functional simulation in later verification steps.

Initially, Layout versus Schematic (LVS) verification and DRC were run on each individual modules. The LVS checks that the netlist in the original Verilog files matches the layout generated. This tool was crucial in discovering that the

'GND' and 'gnd' nets were not connected and therefore the correction after the synthesis had to be added. The DRC uses a set of libraries supplied by XFAB to verify that the layout is within their manufacturing parameters.

In order to simulate each module a schematic with function generators to drive the inputs of each module was created. The simulation was run at different abstraction levels, starting with a functional simulation which verified that the VHDL code and the top-level schematic were correct. The simulation was then run using cmos_sch, which simulates the circuit at a transistor level. This type of simulation is much slower and it was not practical to fully simulate the complete logic with serial interface; however, it was used on the other segments with individual circuit modules, to more accurately verify that the circuit met the timing constraints.

4.2.3 Detailed description of the silicon modules

4.2.3.1 Silicon module 1: the full micro-mirror closed loop controller including debugging interface

The complete controller module (numbered (1) in Figure 4-2), consists of the following:

- Amplitude and phase measuring block
    - Pulse timing measurement using running counter
    - Lookup tables
    - Mirror oscillation detector
    - Phase error and amplitude error calculation
- Output signal generator
    - Mirror oscillation starter
    - Duty cycle control
    - Frequency control
    - Dithering frequency generator

- Serial interface
    - Serial data decoder
    - Serial data encoder
    - BCD generator
    - UART interface

Figure 4-5 shows a block diagram of the controller as used to operate the resonating micro-mirror. The controller inputs consist of the feedback from the high voltage drive signal and the photodiode laser sensing circuit, and its output drives the high voltage amplifier that actuates the micro-mirror. The feedback signals are used to measure the amplitude and phase using the technique described in Section 3.3 of this thesis. The amplitude and phase signal are used to computed the amplitude error and phase error which are used by the controller to adjust the output frequency synthesiser. The frequency synthesiser uses the dithering technique described in Section 3.4 to generate a precise output frequency while the PWM technique described in Section 3.6 adjusts the duty cycle of the output.

The serial interface is used (i) to adjust the operating parameters of the controller and update the lookup table and (ii) for debugging purposes.

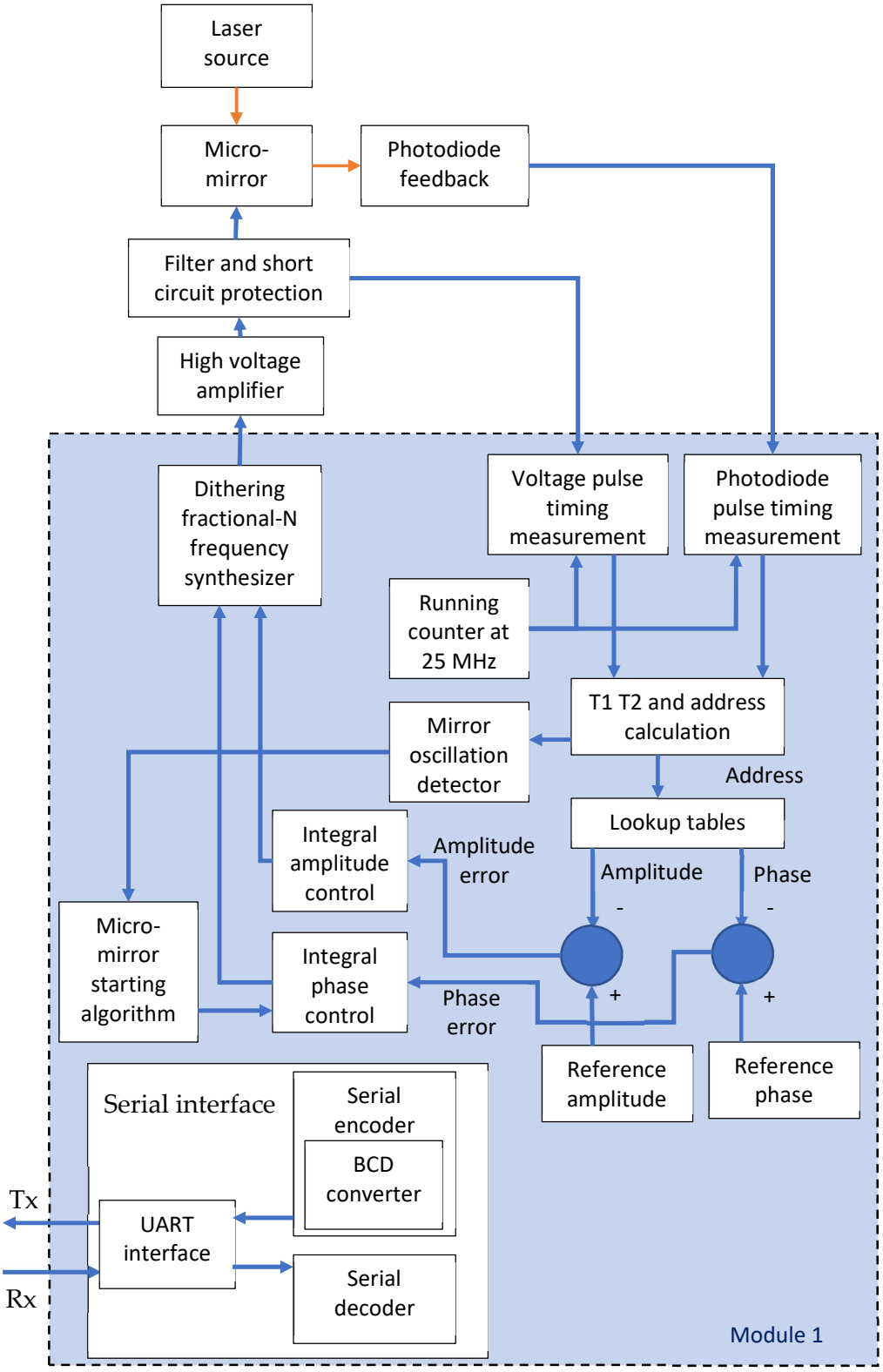

Figure 4-5: Silicon module 1: full micro-mirror controller, highlighted in blue.

The amplitude and phase measurement module implementation is similar to the implementation on the FPGA in Section 3.2, where a running counter is used to measure the timing between pulses. The counter clock frequency is chosen at 25 MHz as a balance between the timing resolution and the limitations of the technology. Choosing a higher frequency results in accuracy frequency, however, it becomes more difficult to obtain a positive WNS and TNS in the layout optimisation stage. Through experimentation it was found that 25 MHz results in a high enough accuracy while being able to achieve positive WNS and TNS. The timing measurements are then used together with lookup tables to compute the phase and amplitude of the micro-mirror oscillations. These values are then translated into commands which are sent to the signal generator which then increments or decrements both the frequency and the duty cycle accordingly. As described in Section 3.2, the implementation includes distributed Random Access Memory (RAM) used to store the lookup tables for computing the phase and amplitude. This RAM is initialised from a Read Only Memory (ROM) block and can be updated using the serial interface. Adequate micro-mirror oscillation amplitude is confirmed by a circuit which checks for the presence of the two pulses, referred to in Figure 3-7 (Section 3.3), being generated by the photodiode sensor for every oscillation. This is achieved by checking that the time between the pulses is longer than 0.75 times the period of the driving waveform. If oscillations are detected a digital flag is set.

The drive signal generator block consists of a dithering fractional-N frequency generator described in Section 3.4, together with duty cycle and frequency control described in Sections 3.5 and Section 3.6. The duty cycle and frequency control block use the outputs from the amplitude and phase measurement block in order to adjust the frequency generator parameters and thus forming a closed loop controller. When the oscillating flag is false, the block operates in open loop mode and sweeps the output frequency up and down between two

predefined frequencies in order to initiate the oscillations. This operation is explained in more details in Section 3.5.

The serial interface is used to adjust the parameters of the controller and update the lookup table. The protocol used for serial interface is TTL-RS232 with a baud rate of 115200 bits/s. A USB to TTL adapter is used to interface the signal to a computer. The data is transmitted in ASCII commands with the commands available shown in **Error! Reference source not found.**. Some commands have both an opcode and an operand, where the operand consists of a variable length number in ASCII characters. When a 'c' command is sent from the computer to the controller, a reply is generated which consisted of the parameters shown in Table 4-3. This data can be used to debug the system and record the micro-mirror phase and amplitude.

Table 4-2: List of commands used to update micro-mirror controller parameters through the serial interface.

Command	Description
r\n	Reset
s[x..]\n	Set the target amplitude
e[x..]\n	Increment Duty cycle by operand x
f[x..]\n	Increment Duty cycle by operand x
g[x..]\n	Decrement frequency by operand x
h[x..]\n	Increment frequency by operand x
l[x..]\n	Set the lower frequency in the micro-mirror start up process
m[x..]\n	Set the upper frequency in the micro-mirror start up process
p[x..]\n	Set the amplitude lookup table write address to x
q[x..]\n	Write amplitude lookup table data x
n[x..]\n	Reply with amplitude lookup table value at address x
u[x..]\n	Set the phase lookup table write address to x
v[x..]\n	Write phase lookup table data x
w[x..]\n	Reply with phase lookup table value at address x
c\n	Reply with parameter list

Having this serial interface allows the use of the micro-mirror controller in open loop mode. In this mode the frequency and duty cycle can be incremented or

decremented manually and therefore used to evaluate the micro-mirror performance at specific operating points. In a practical application this can be used to find the mechanical frequency of oscillations.

In closed loop mode parameters such as the range of frequency to scan when starting the micro-mirror and target oscillation amplitude can be set.

The complete controller described above was implemented in an area of 1850 μm by 2350 μm. An image of the implementation is shown in Figure 4-6. This render shows the uppermost layer, which is the thick metal layer, of the implementation. Table 4-3: List of parameters sent from the controller over the serial interface

Message line number	Name	Description
1	Voltage period	Used to calculate the output frequency
2	Duty cycle	Used to calculate the output duty cycle
3	T2	T2 in Figure 3-7
4	Amplitude	Measured amplitude of the micro-mirror
5	phase	Measured phase of the micro-mirror
6	T1	T1 in Figure 3-7
7	T1_T2	T1 + T2 used to measure the micro-mirror frequency
8	Target upper limit	Lowest frequency of the micro-mirror start-up procedure
9	Target lower limit	Highest frequency of the micro-mirror start-up procedure
10	Phase error	Measured phase error
11	Voltage high	Running counter at voltage rising edge
12	Counter 3	Running counter value
13	Addr3	Lookup table read address
14	Inst temp phase	Lookup table phase readout

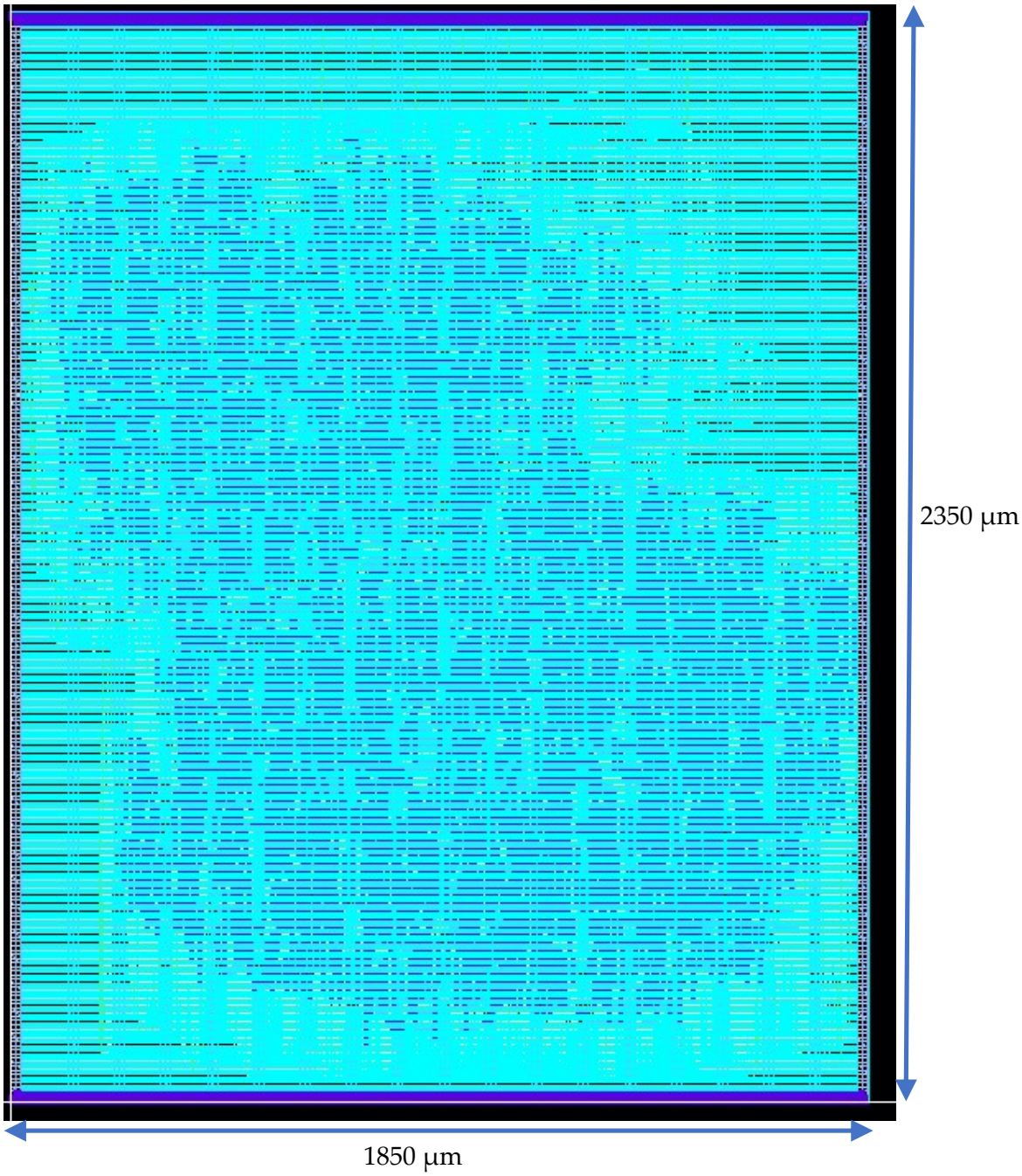

Figure 4-6: Implementation of the whole micro-mirror controller including serial interface for debugging as seen from uppermost metal layer

4.2.3.2 Silicon module 2: amplitude and phase measuring logic

The amplitude and phase measuring block described in the Section 4.2.2.1, is again implemented on its own in this module, numbered (2) in Figure 4-2, with

a block diagram of the implemented module shown in Figure 4-7. The main difference is that the parameters are all set as constant and the lookup table is external to the ASIC. The implementation of the external lookup tables is also kept as simple as possible by using a parallel bus for both the address and the two data signals. This was done intentionally to avoid the complexity of a serial bus which would reduce the number of pins needed but at the same time increase the risk of something going wrong. This means that the area used is much smaller and the block overall is simpler and therefore there was less risk that problems arose. The main drawback is that since the lookup tables are implemented externally using a parallel bus, a large number of pins are needed. This module is implemented in an area of 1350 μm by 150 μm and a render of the top layer is shown in Figure 4-8.

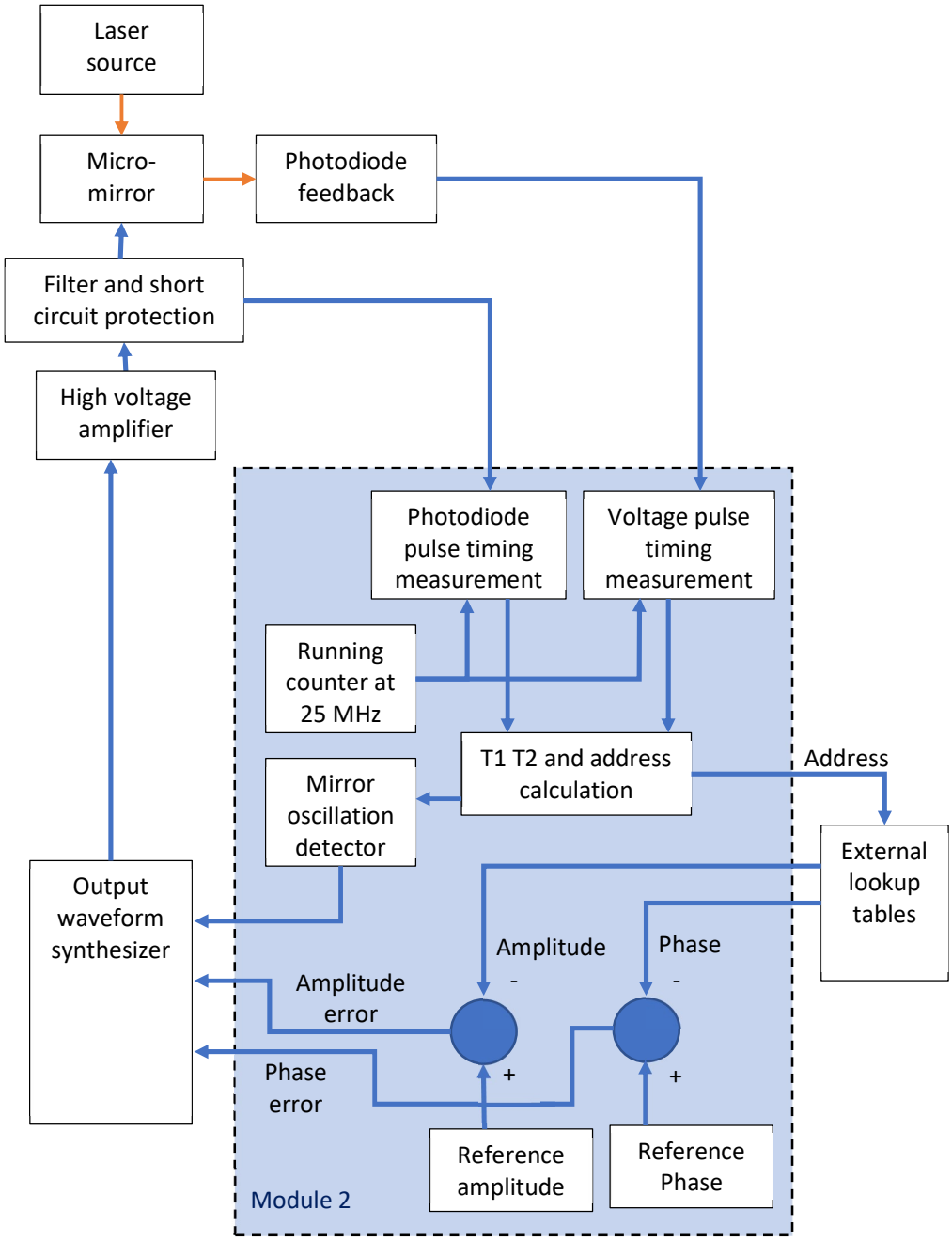

Figure 4-7: Amplitude and phase measuring block diagram highlighted in blue.

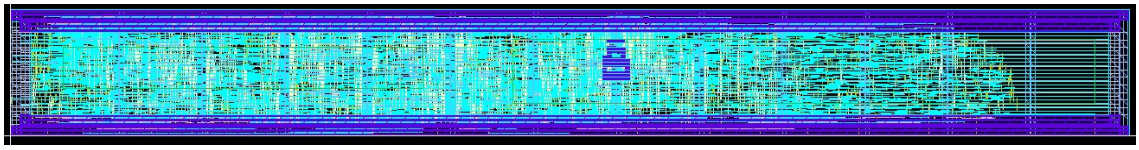

Figure 4-8: Amplitude and phase measuring logic implementation

4.2.3.3 Silicon module 3: drive signal generator

The drive signal generator block described is Section 4.2.2.1 is again implemented on its own in this module and numbered (2) in Figure 4-2. The implemented blocks are shown in Figure 4-9. In this case the parameters are all implemented as constants in order to simplify the overall implementation. This reduces the risk of errors in the implementation and allows the block to be tested on its own.

The total area required by the block was 450 μm by 250 μm. Figure 4-10 shows the overall area of the drive signal layout, with the power rings at the edges, the power stripes and the top layer connects.

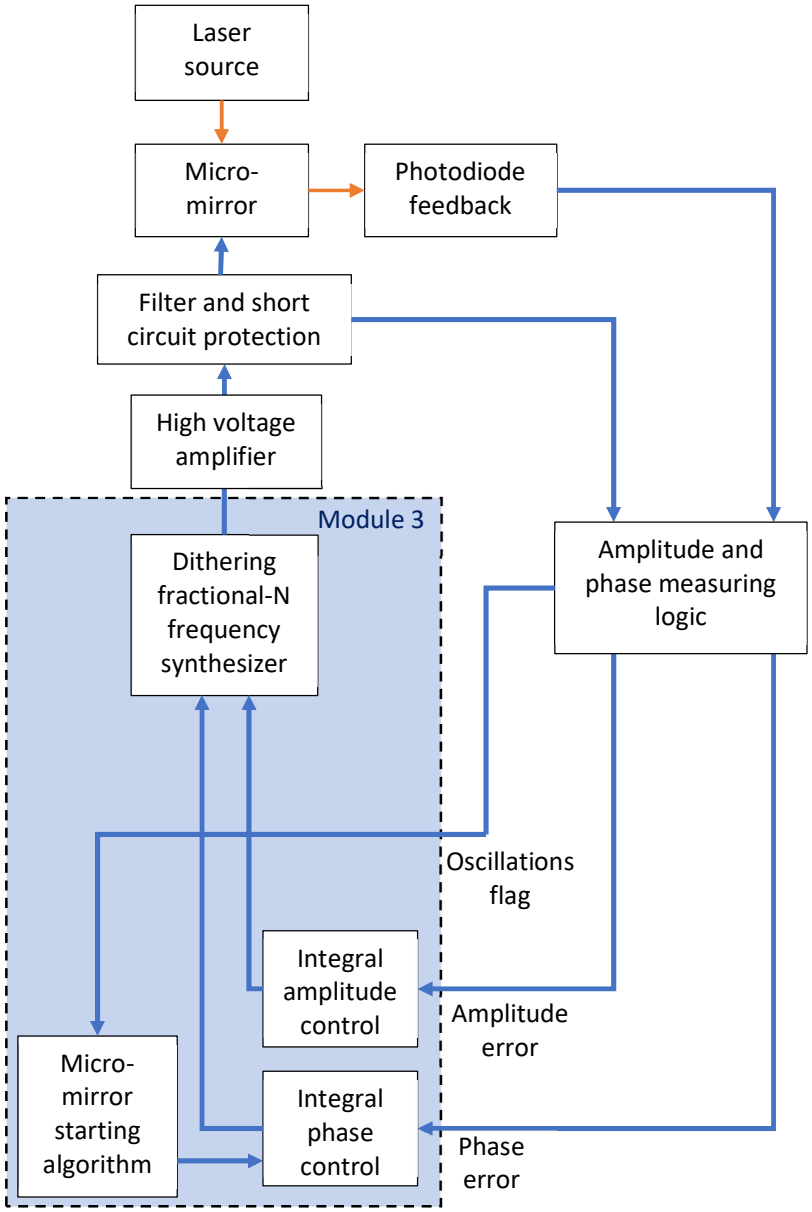

Figure 4-9: Drive signal generator block diagram highlighted in blue.

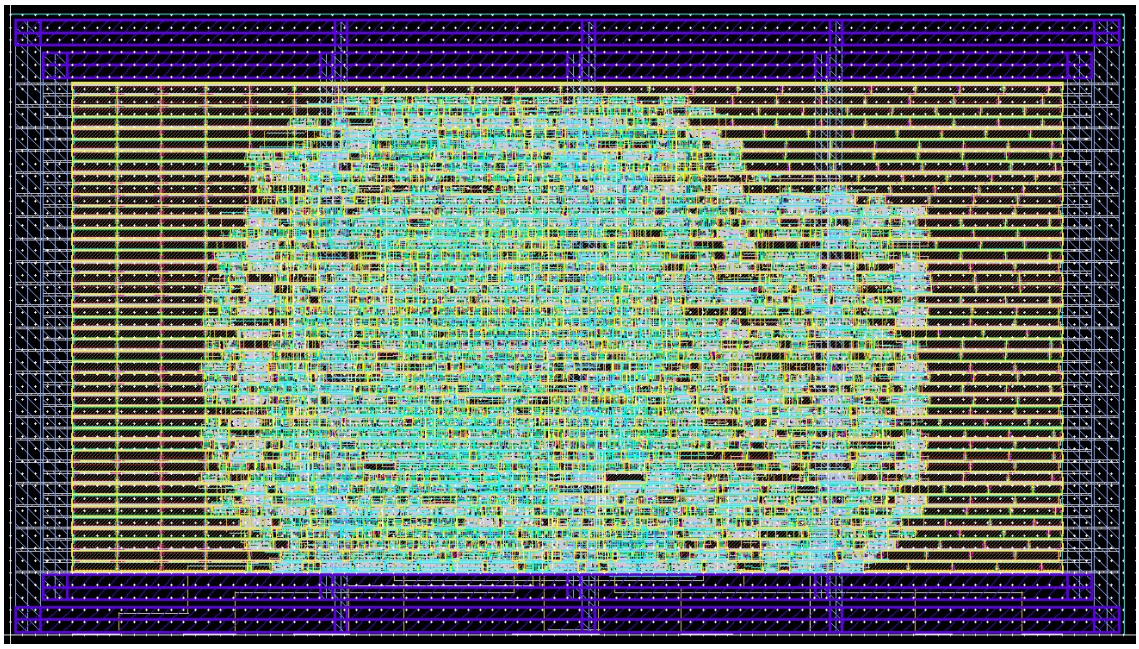

Figure 4-10: Drive signal generator implementation

4.2.3.4 Silicon module 4: debounce logic

The amplitude measuring circuit uses the timing of pulses from a photodiode in line of a reflected laser beam. This circuit is sensitive to any oscillations present during the rising edge. This problem becomes more evident when the circuit is used in a laboratory setup using coaxial cables to interface the various components of the system. To mitigate this issue two debounce circuits numbered (4) in Figure 4-2 were implemented, one for the photodiode signal and one for the voltage signal feedback.

The debounce logic synchronises the input signal with the input clock, updates the output and then ignores input changes for the following 320 ns, that is the input clock period (40 ns) multiplied by 8. This is implemented using the code presented in appendix 3. The circuit synchronises the input signal to the system clock by buffering the signal in a clock triggered process. When an input changes the output is updated accordingly, a counter is started, and any further

output updates are blocked. This counter steps up to eight before resetting and new output updates are unblocked.

Two identical instances of the module were implemented so that any delay introduced to the photodiode signal and voltage signal are identical. The physical layout, produced by cadence Innovus tool, implementing the VHDL code of the debounce logic is shown in Figure 4-11. The area used by the debounce logic, excluding the power rings, is 33 μm by 33 μm.

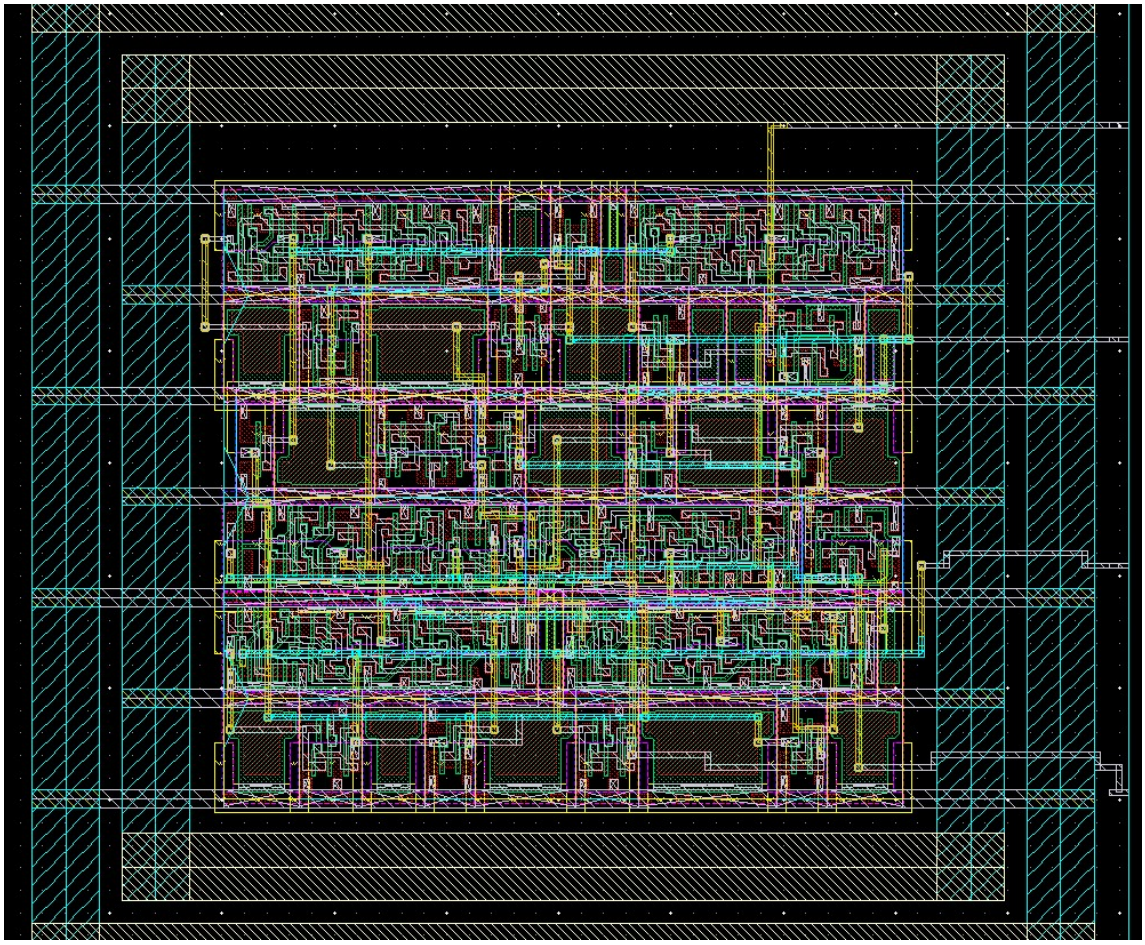

Figure 4-11: Debounce logic implementation

4.2.3.5 Silicon module 5: high voltage micro-mirror driver circuit

Since the micro-mirror being used for testing uses electrostatic actuation, a high voltage, typically between 100 V and 200 V, is required for its operation. A push pull configuration was chosen as the high voltage driver. A level shifter was needed to operate the high side P-channel MOSFET as shown in Figure 4-12. A conventional voltage level shifter was used [81]. Two bias voltages were added to limit the level shifter output voltage swing to prevent damage to the gates of the output MOSFETs. The bias voltages are connected to external pins so that they can be adjusted depending the supply voltage used.

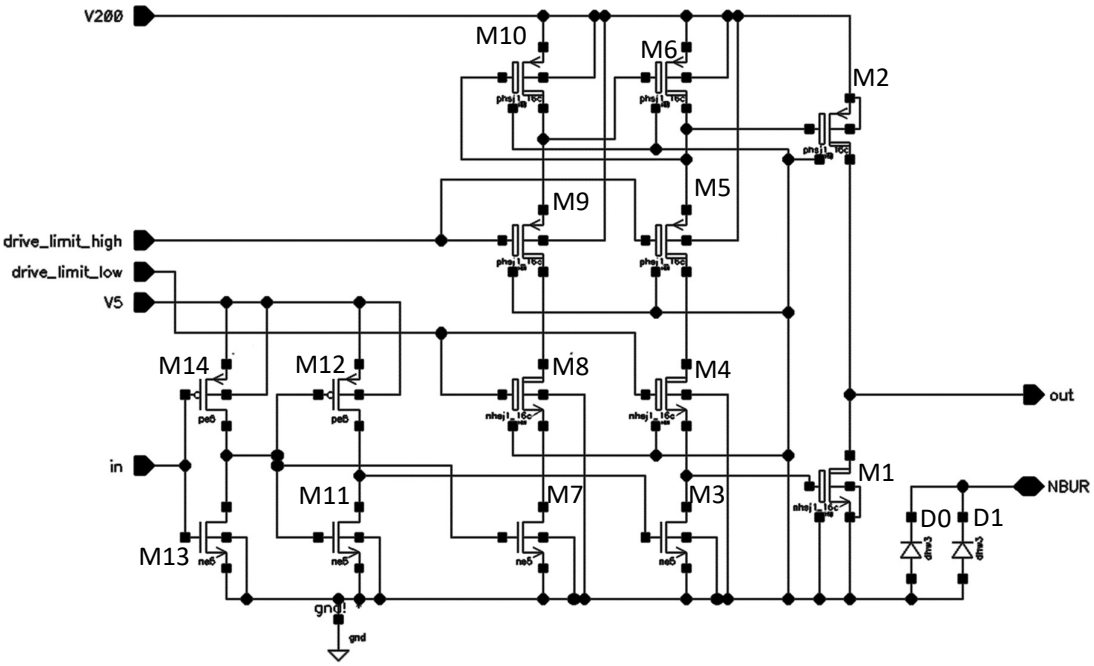

Figure 4-12: High voltage drive circuit, silicon module 5

The circuit was simulated using Cadence Virtuoso ADE Suite Verifier [82] . This software was set up to carry out transient simulations in order to evaluate the rise time, fall time, and voltage levels of the output waveform.

The simulation results are shown in Figure 4-13. A capacitance load of 100 pF was used for simulation; however, this does not necessary represent the typical load of an electrostatic micro-mirror which typically has an input capacitance of less than 10 pF. For the simulation a larger capacitance was used to emulate the worst-case condition where coaxial cables are used during laboratory testing.

For a load capacitance of 100 pF and taking a rise time of 1 μs, a current of approximately 20 mA is needed. The N-channel datasheet shows a worst-case saturation current of 71 μA/μm. From this a minimum gate width of 281 μm is needed. This does not consider the on-resistance of the MOSFET and the cabling involved. For this reason, the gate width of the transistor was increased to 400 μm. The P-channel MOSFET has a worst-case saturation of 40 μA/μm, which is approximately half than of the N-channel. Therefore, its gate width was chosen to be double at 800 μm. Simulation results show a rise time of 0.36 μs and fall time of 0.38 μs, with a peak discharging current of 62 mA during the falling edge and charging current of 80 mA during the rising edge. These values are shorter than the target of 1 μs.

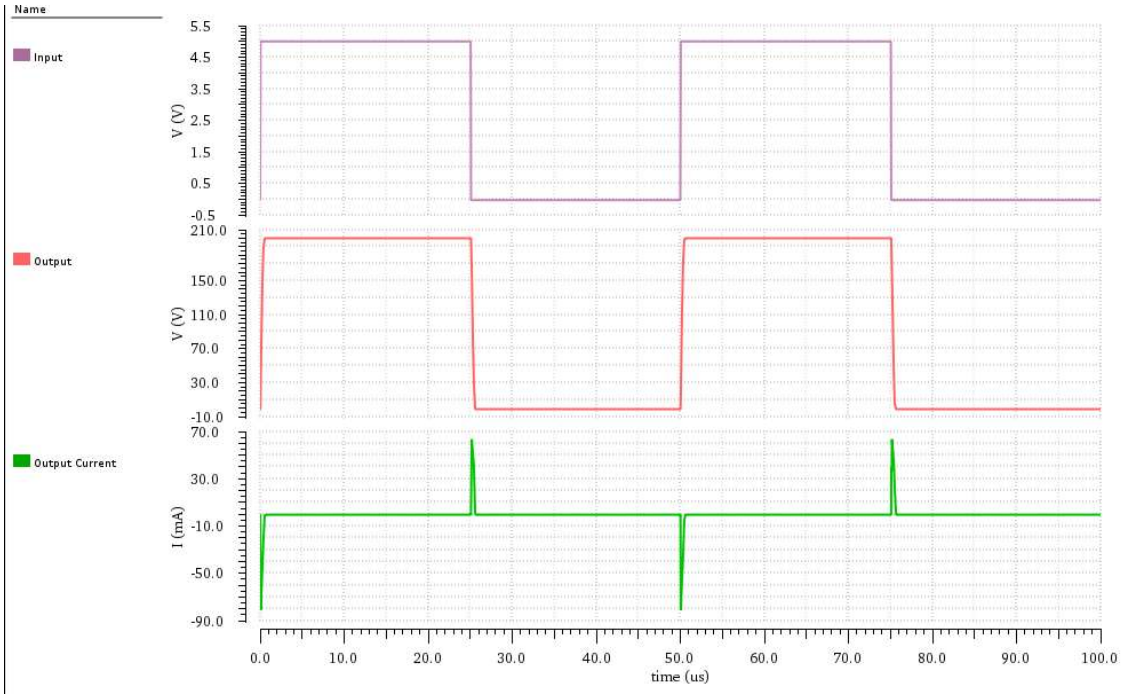

Figure 4-13: Simulation of high voltage drive circuit

4.2.4 High voltage micro-mirror driver implementation

The high voltage driver was implemented using XFAB XT018 200V HV PMOS and NMOS devices. In order to isolate the high voltage MOSFETS from the substrate, they were placed in an n-well using a specialised diode. The isolated n-wells are created using diodes D0 and D1, which are 200V diodes that extend to below the buried oxide layer. When reverse biased, these diodes isolate a section of the wafer from the remaining wafer and therefore stop any leakage current from the high voltage MOSFETS to the handle wafer contact. Special pads with 200 V Zener protection were used for the high voltage pins.

The total area of the high voltage drive implementation excluding the protection diode is 660 μm by 378 μm. An image of the layout is shown in Figure 4-14.

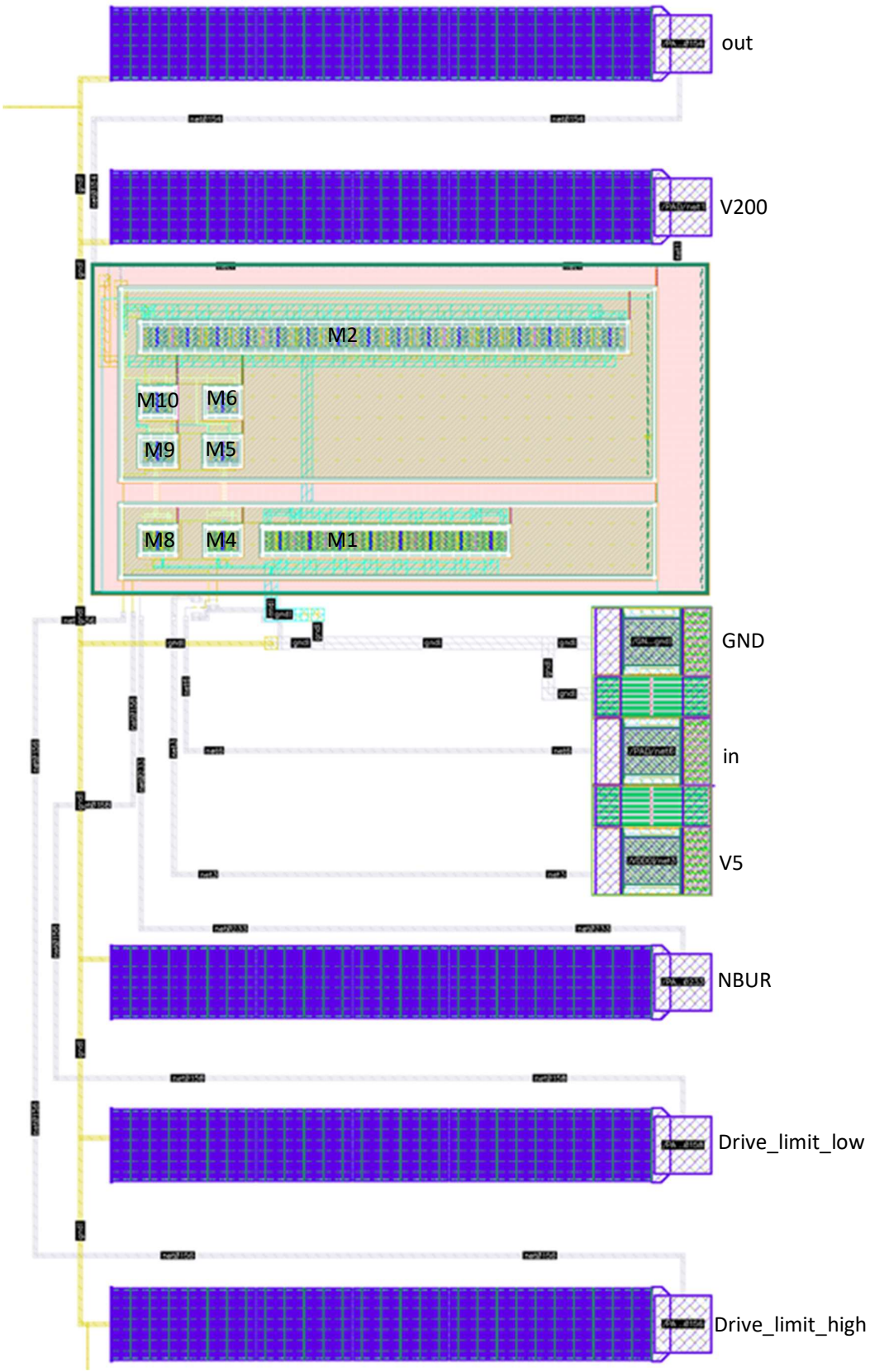

Figure 4-14: High voltage drive and corresponding pins implementation.

4.2.5 Die layout

The XFAB XT018 under the Europractice agreement has a minimum fabrication cost equivalent to a silicon area of 10 mm^2. This minimum cost area was utilised, with the die area being set to 3026 μm by 3226 μm. This area was found to be adequate for the placement of the pins and the various controller blocks. The high voltage driver and its related pins were placed in the top right-hand corner. The remaining segments were distributed as shown in Figure 4-15, with pins along the outer edge [74]. A micro-photograph of the manufactured die is shown in Figure 4-16.

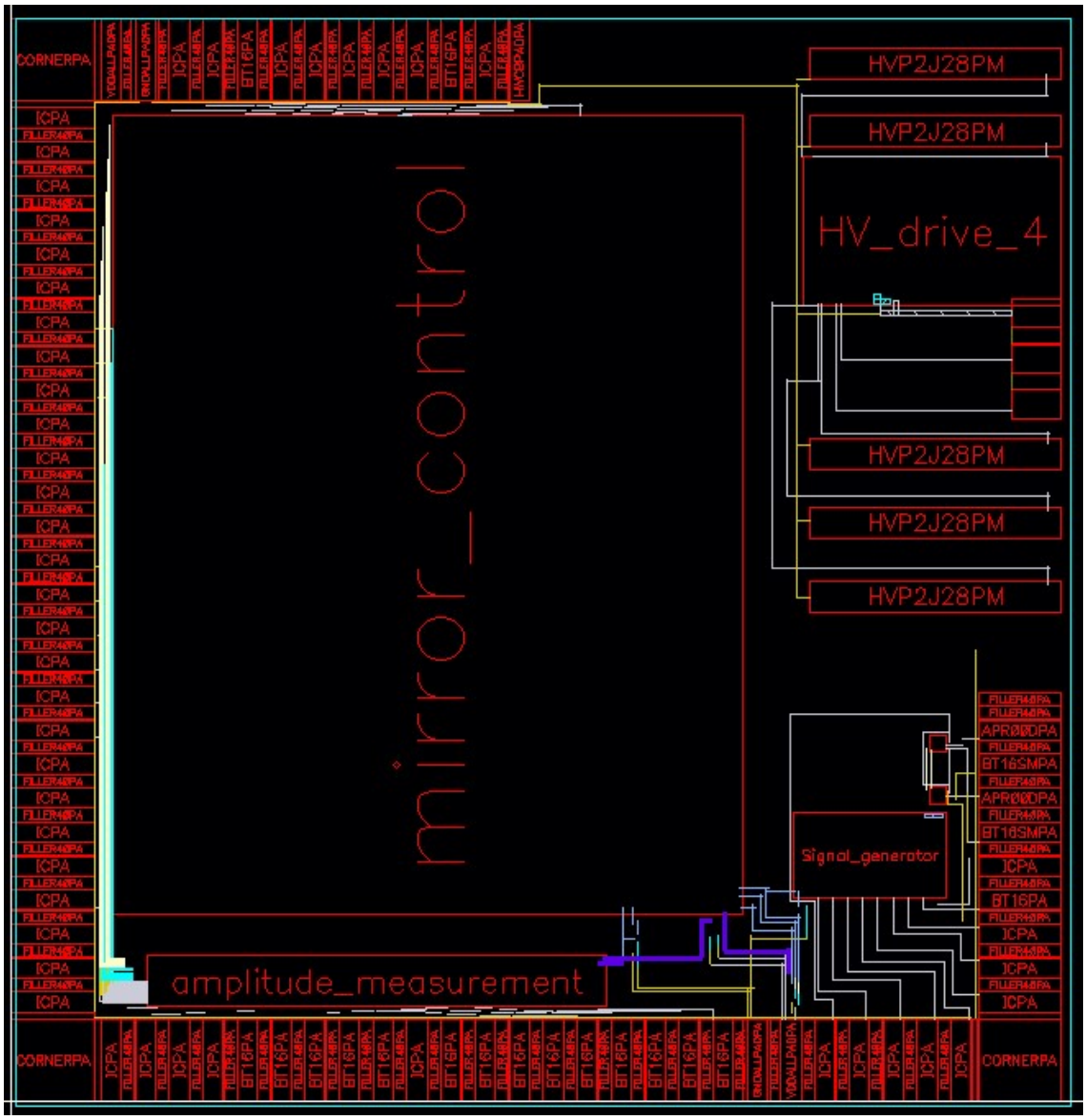

Figure 4-15: Die layout

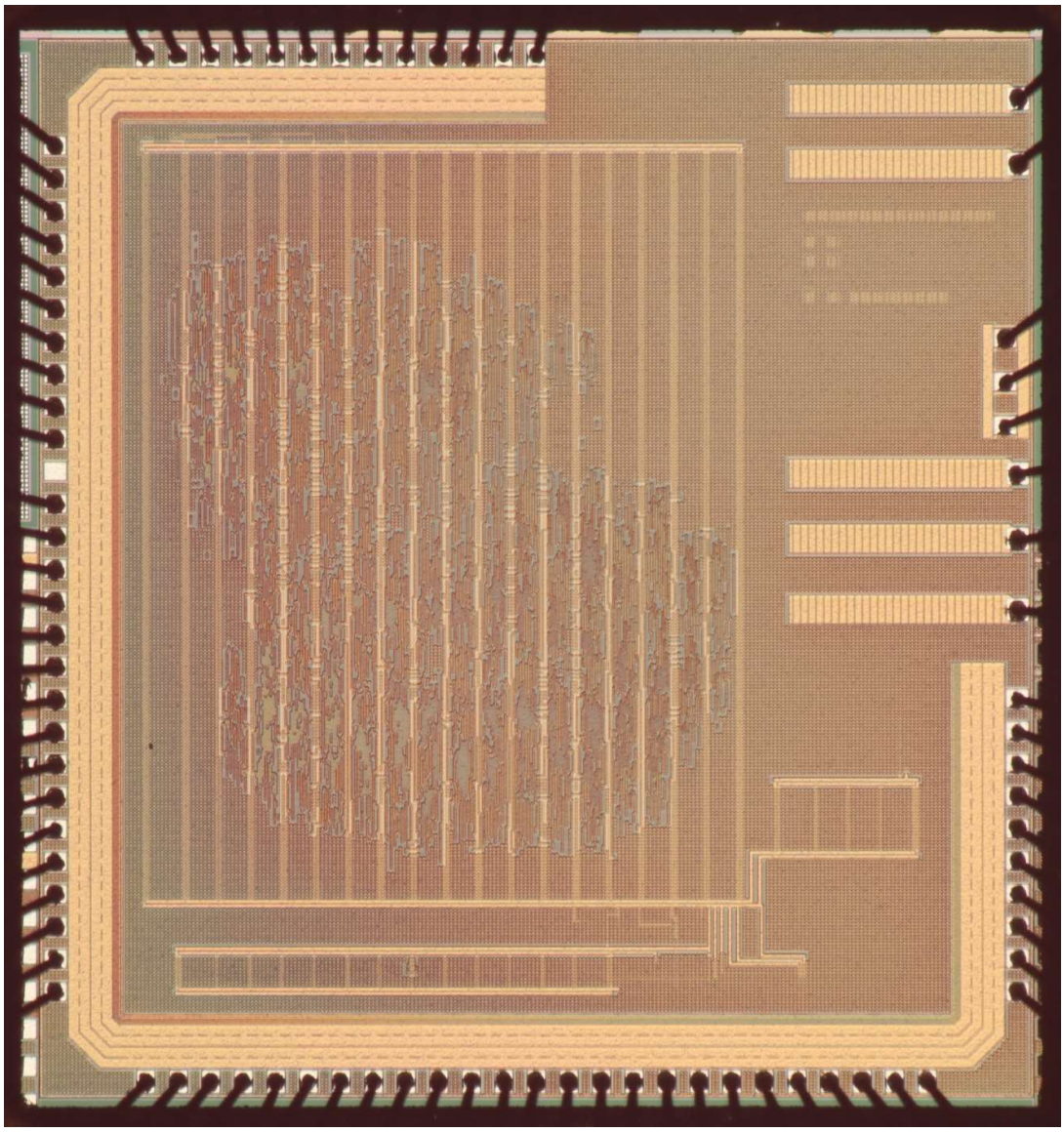

Figure 4-16: Micro-photograph of the manufactured die

4.2.6 IC Package

A total of 50 dies were fabricated at X-FAB facilities, of which 25 were bonded in a CPGA120 package as per bonding diagram shown in Figure 4-17. An image of the manufactured IC is shown in appendix 4.

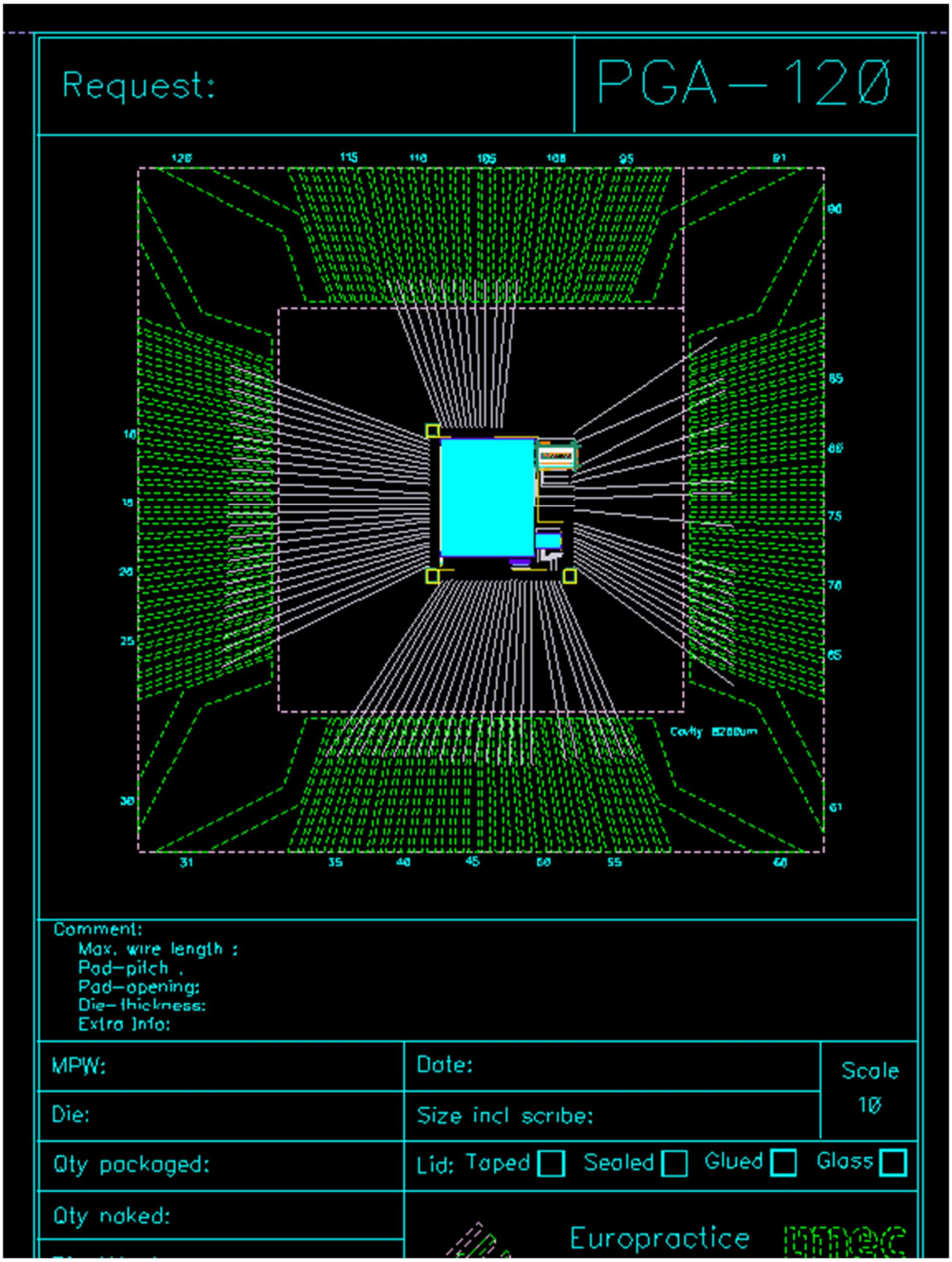

Figure 4-17: Bonding diagram

4.3 Conclusion

The digital controller and high voltage driver are implemented on an ASIC as a demonstration of the feasibility of such an implementation. The implementation is divided in modules so that individual modules can be tested independently. This reduces the chance that if a block does not function as intended, testing could still be carried out on the remaining blocks. Moreover, the digital controller implemented is duplicated in two approaches: with an integrated serial interface that enables real time monitoring of the controller status and updating of the controller parameters, and as pre-programmed blocks with external flash. The latter is more representative of a commercial implementation which does not require the added debugging components.

A unipolar high voltage square wave generator is also implemented in the design. This circuit uses the high voltage MOSFETs available in the XFAB XT018 BCD-on-SOI process which are designed to handle a drain to source voltage of 200 V. The design demonstrates that the high voltage driver can be implemented on the same die and thus that a whole micro-mirror controller can be implemented in a single device.

The ASIC incorporating the novel control systems and integrated with the high voltage driver was manufactured through the Europractice platform and a total of 25 dies were packaged in a PGA120 package.

5 Characterisation setup and testing results

The micro-mirror controller was tested via the optical setup available at the University of Malta optical characterisation lab consisting of a position sensitive detector (PSD), a laser source and a beam splitter cube. The optical setup is placed in a blackout enclosure to remove interference from ambient light. The aim of the setup is to evaluate the performance of the micro-mirror controller and compare the individual ASIC building blocks with previous results obtained using the FPGA platform and benchtop high voltage amplifier.

The first tests were carried out on the complete controller described in Section 4.2.2.1. This block includes the closed loop amplitude and phase controller together with the required lookup tables and debugging over serial interface. The testing was carried out by first verifying that the serial interface and various outputs were operating correctly and followed by comparing the oscillation amplitude measured using a PSD against the amplitude set through the serial interface. The testing was repeated for the amplitude and phase measuring block described in Section 4.2.2.2 and drive signal generator block described in Section 4.2.2.3. The two blocks were connected together and the lookup tables needed for computing the amplitude and phase are implemented externally, in this case on an FPGA which emulated a parallel flash memory module.

Following the verification of the digital logic, the high voltage bench top amplifier was replaced with the embedded high voltage circuit on the ASIC. The high voltage circuit was powered from an external high voltage power supply and the performance of the amplifier in driving the micro-mirror was evaluated.

5.1 Testing setup

The optical setup shown in Figure 5-2 was used to evaluate the controller performance. A Thorlabs HNL020LB helium-neon laser source [83] and a Thorlabs P500HK 0.5 mm pinhole [84] are used as the stable and collimated laser beam. A Thorlabs BS010 10 x 10 mm 50:50 beam splitter cube [85] is used to split the laser beam in two directions with one of the beams intersecting the micro-mirror. The laser beam is reflected back through the beam splitter cube and again split in two: one beam intersects a PSD sensor, while the other beam intersects the photodiode used for amplitude and phase measurement. The use of the beam splitter cube allows for the concurrent micro-mirror angle measurement using a PSD and using the proposed single photodiode technique. The PSD is a high precision laboratory sensor consisting of a Hamamatsu C10443-04 [86] and has a detection area of 12 x 12 mm. Due to limitations caused by the beam splitter cube size and PSD detection area, the maximum oscillation amplitude that can be measured is limited to 17°.

The signals from the PSD are recorded to MATLAB using a Picoscope 5444B and in order to determine the amplitude of the projected laser line. The amplitude measurement from the proposed single photodiode measurement system is transferred to MATLAB using the serial interface described in Section 4.2.2.1.

The layout of the optical path is shown in Figure 5-1 and an image of the actual setup placed in an optical blackout enclosure is shown in Figure 5-2. This characterisation setup is related to the diagram shown in Figure 3-7 in Section 3.3. The original distance y_0 referred to in Section 3.3 is equivalent to the summation of y_1 and y_2 shown in Figure 3-7.

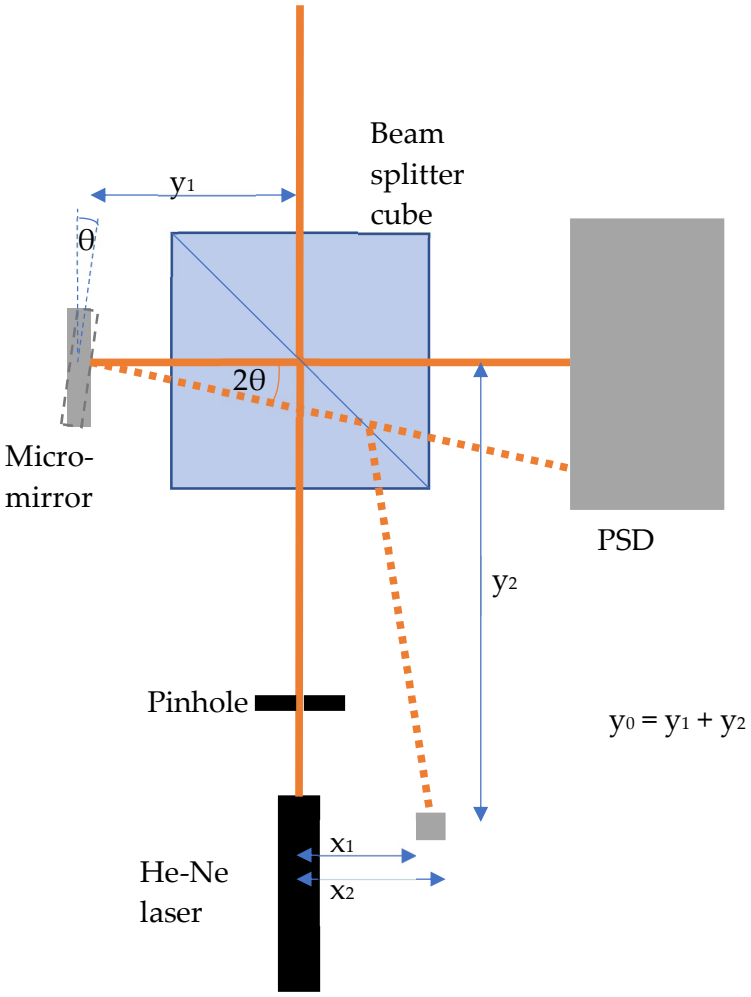

Figure 5-1: Layout of the optical path

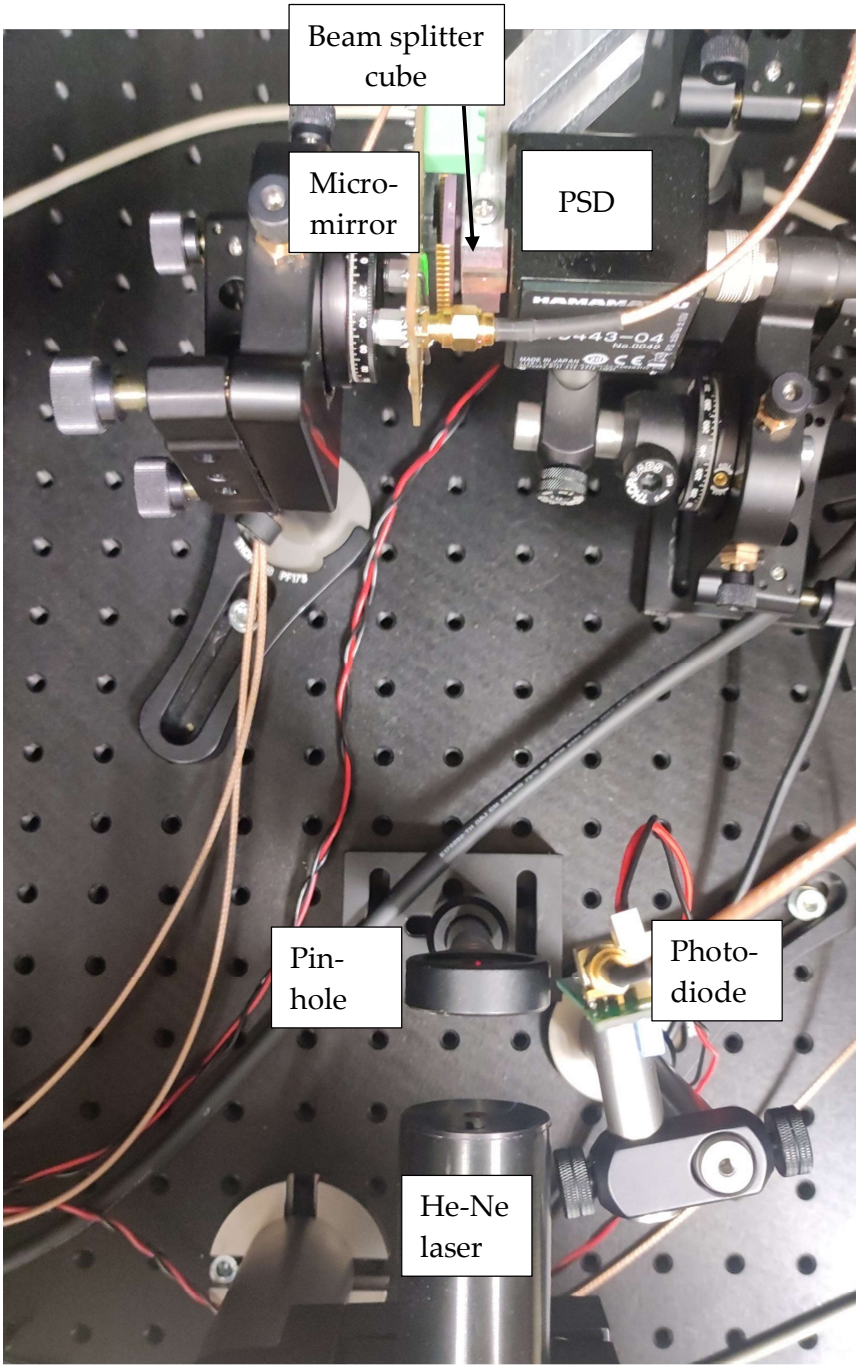

Figure 5-2: Optical setup used for testing the micro-mirror controller

5.2 PCB design

Two PCBs were designed and manufactured while the ASIC was being manufactured. These are used as breakout boards for verifying the different

ASIC building blocks. The first board, shown in Figure 5-3 is used for testing the complete controller and the analogue high voltage driver. The second board, shown in Figure 5-4, is used to test the independent implementation of the amplitude and phase block and the drive waveform synthesis block. The boards feature SMA connectors which are used to interface the controller with the micro-mirror using coaxial cables. The second board uses a VHDCI connector to interface the ASIC to external lookup tables via a parallel bus. For testing purposes, an FPGA is used to emulate the external flash lookup table containing key parameters for estimating the amplitude and phase of the micro-mirror. The lookup tables details are presented in Table 3-1 in Section 3.3. During the complete ASIC testing the internal lookup tables are utilised and no FPGA support is required. The board includes a linear regulator which drives the ASIC at 1.8 V. Details and photos of the manufactured PCBs can be found in Appendix 5.

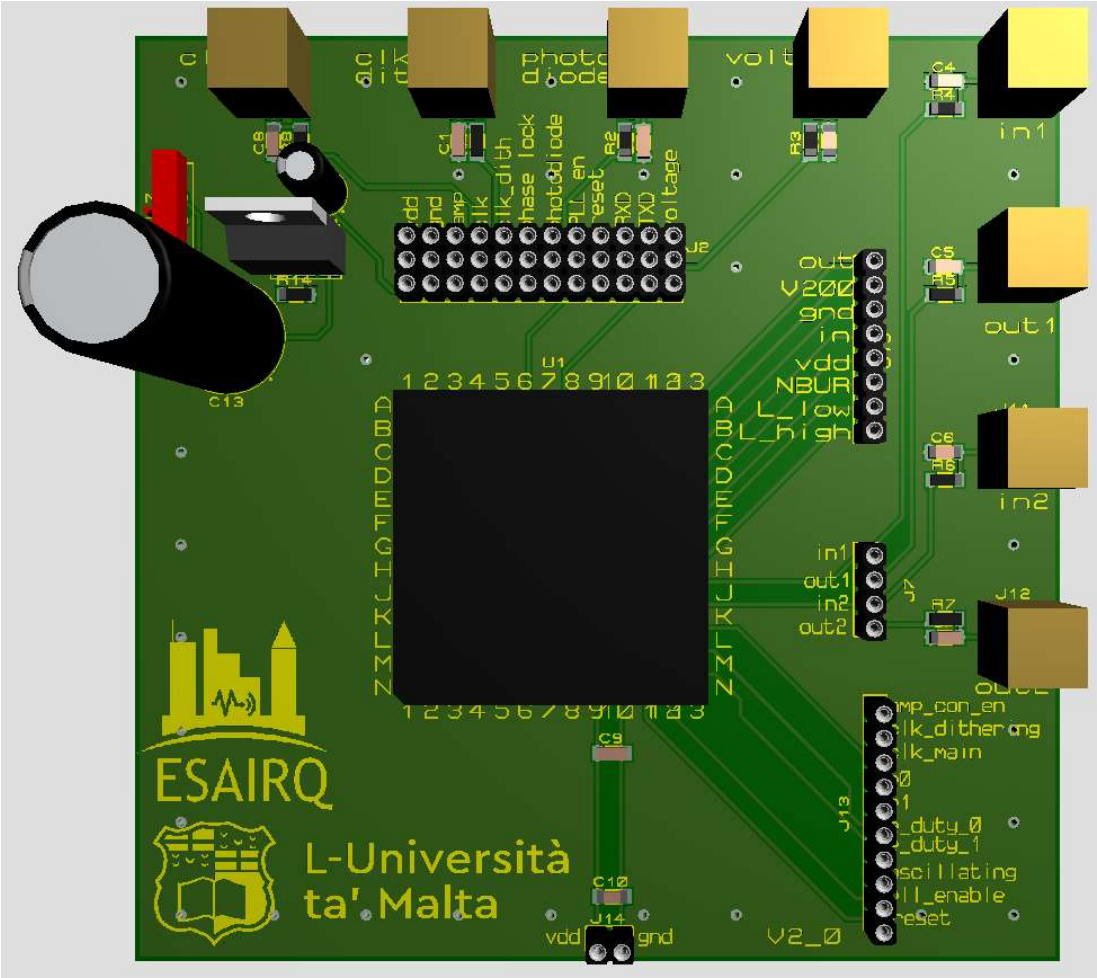

Figure 5-3: Primary board used to test the whole controller with serial interface and high voltage driver

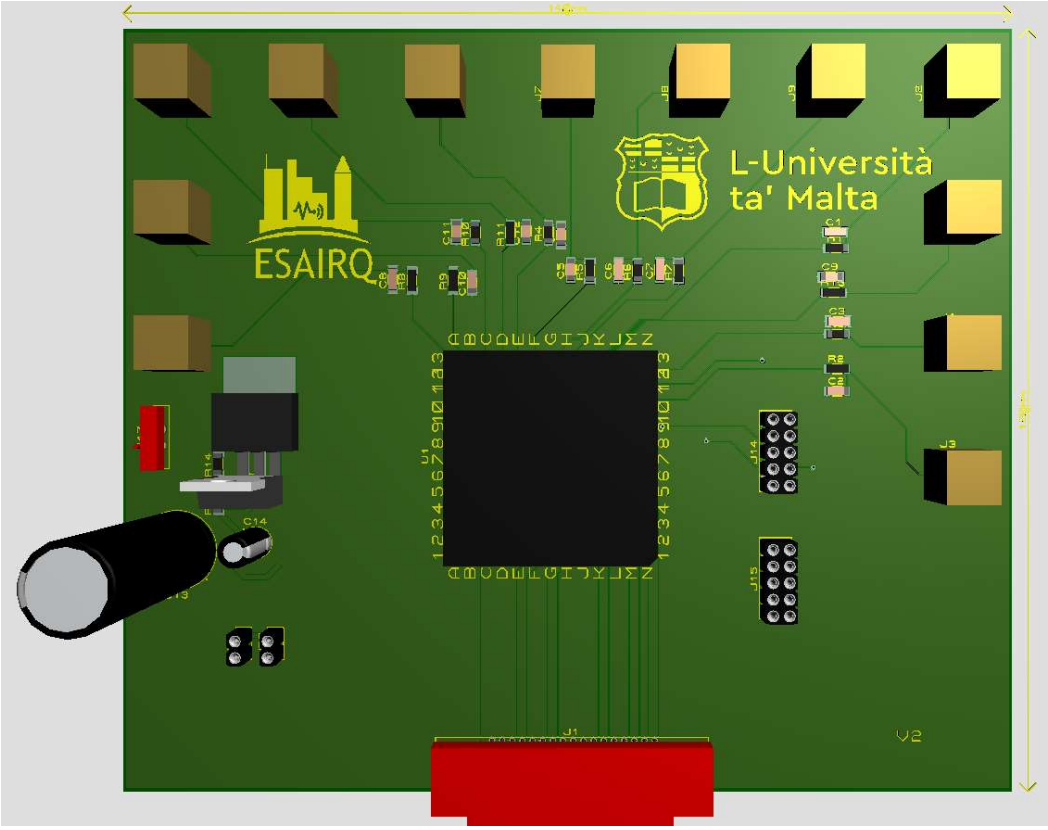

Figure 5-4: Secondary board used to test independent sub systems of the controller

5.3 Low voltage testing of the digital controller

The ASIC implementation was installed in the test setup in place of the FPGA controller discussed in Chapter 3. A block diagram of the test setup and ASIC is shown in Figure 5-5. The ASIC supply voltage is set to 1.8 V and is driven by a clock frequency of 25 MHz. The first module tested was the serial interface. The Rx and Tx lines of the serial port were connected to a RS232 to USB adapter with level shifters which operated down to the 1.8 V signal levels which are compatible with the ASIC. With a baud rate of 115200, communication was established.

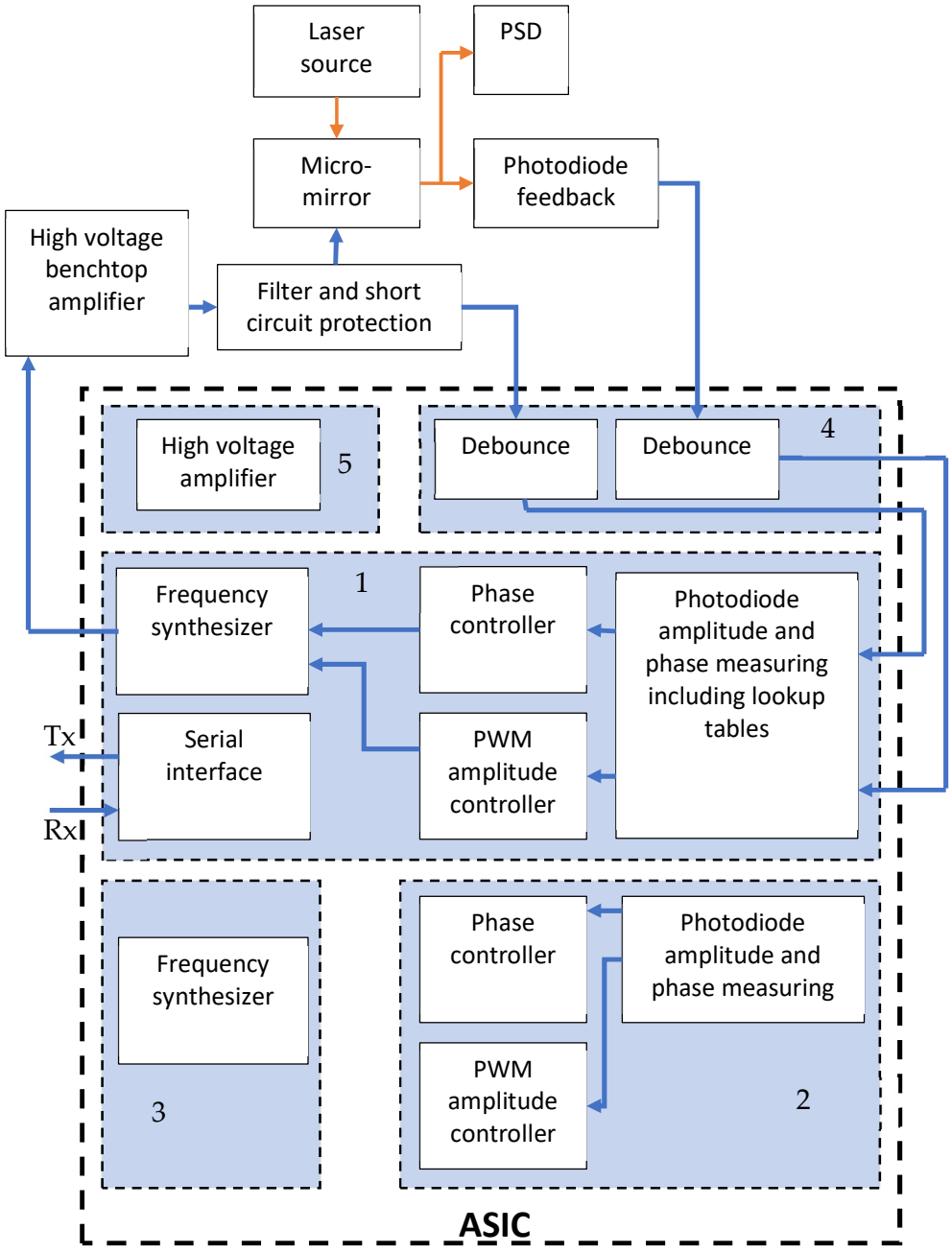

Figure 5-5: Micro-mirror and ASIC block diagram when testing the complete controller

The complete controller parameters described in Section 4.2.2.1 were set up for the 21 KHz AVC micro-mirror via the serial port communication channel. Preliminary tests were carried using only the digital part of the ASIC and a

benchtop high voltage amplifier. Figure 5-6 shows the steady state oscillation amplitude of the micro-mirror as measured by the PSD against the desired angle set on the ASIC. A good agreement was achieved with a maximum error of less than 2.8%. The Root Mean Square Error (RMSE) was calculated to be 1.58% which verifies a good linear relationship between the set maximum angle and measured maximum angle. This is an improvement compared to the RMSE of 1.82% published in [87].

The oscillation amplitude envelope at start up is shown in Figure 5-7. The oscillation amplitude fluctuates slightly during start-up. This behaviour was previously observed analytically and experimentally in Section 3.5. The response takes long to reach steady state as the controller transitions from oscillation start-up mode to closed loop mode: in the start-up mode the output frequency is sweep between two limits until the oscillation amplitude increases to a point where the reflected laser beam intersects with the photodiode feedback. It should be noted that in the FPGA implementation the starting frequency was manually set. This explains the increased start-up time during ASIC characterisation. In the last section of the plot the oscillation amplitude decreases slightly when the PWM amplitude control starts decreasing the duty cycle of the output waveform in order to achieve a stable oscillation amplitude.

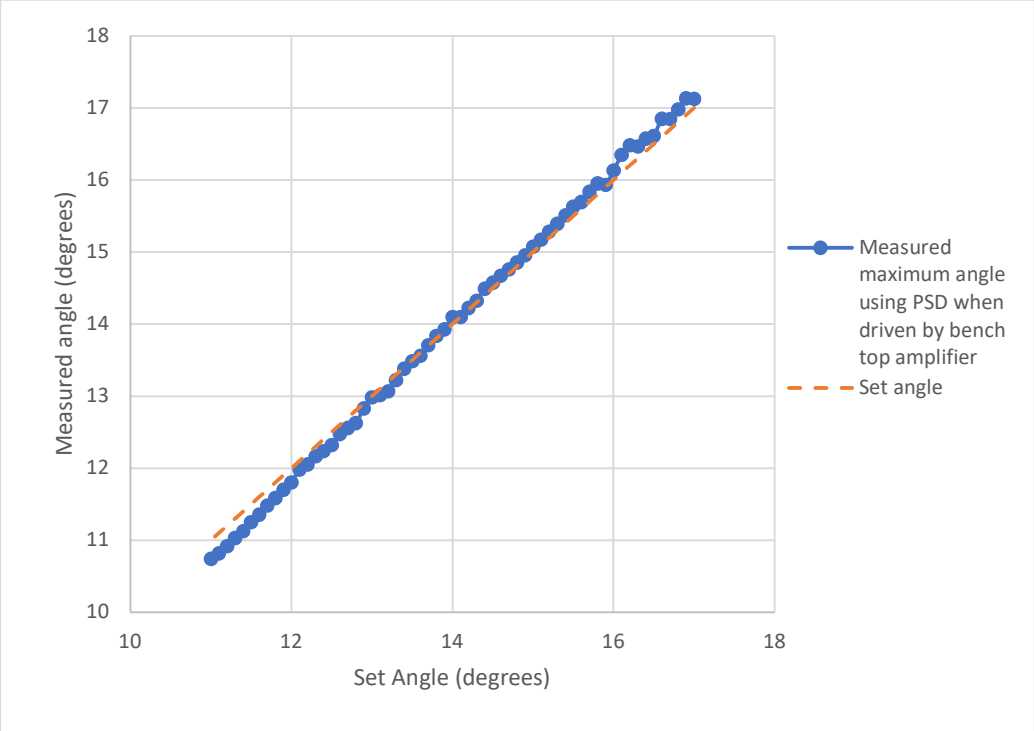

Figure 5-6: Comparing angle set on the ASIC with maximum angle measured using PSD

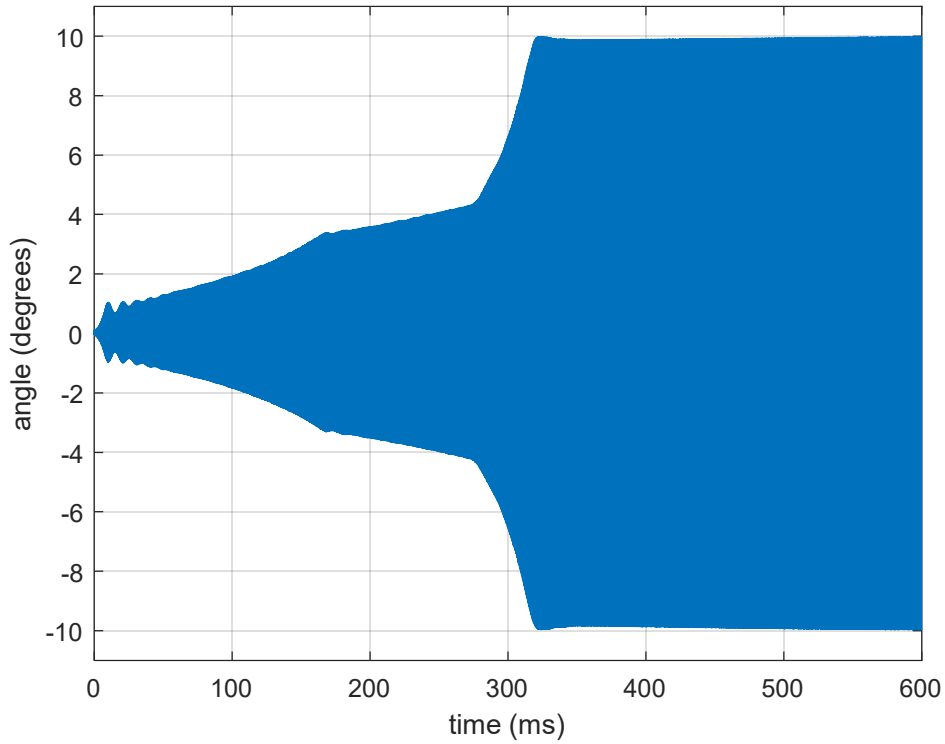

Figure 5-7: Oscillation amplitude envelope at start-up.

5.4 Low voltage testing of the ASIC individual testing blocks.

The same testing carried out on the complete digital controller was repeated on the individual testing blocks described in Section 4.2.2.2 and Section 4.2.2.3. A block diagram of the test setup is shown in Figure 5-8.

For this test the outputs of the amplitude and phase measuring block were connected to the respective inputs of the drive signal generator. Since no serial interface is available in these blocks, all parameters were pre-set at the implementation stage and the amplitude of oscillations is fixed at 15°.

The lookup tables needed for the amplitude and phase measuring block are implemented external to the ASIC. For the testing carried out in this study the lookup tables are implemented on an FPGA which emulates a FLASH memory module. This approach meant that it was rather easy to update the lookup table depending on the optical configuration available.

When powered and with the closed loop control enabled, the two blocks operated the micro-mirror correctly and a stable output oscillation amplitude of 15.07° was measured using the PSD, which is very closed to the set 15°. This demonstrated that the minimised controller implemented in these two blocks is effective in driving the AVC micro-mirror.

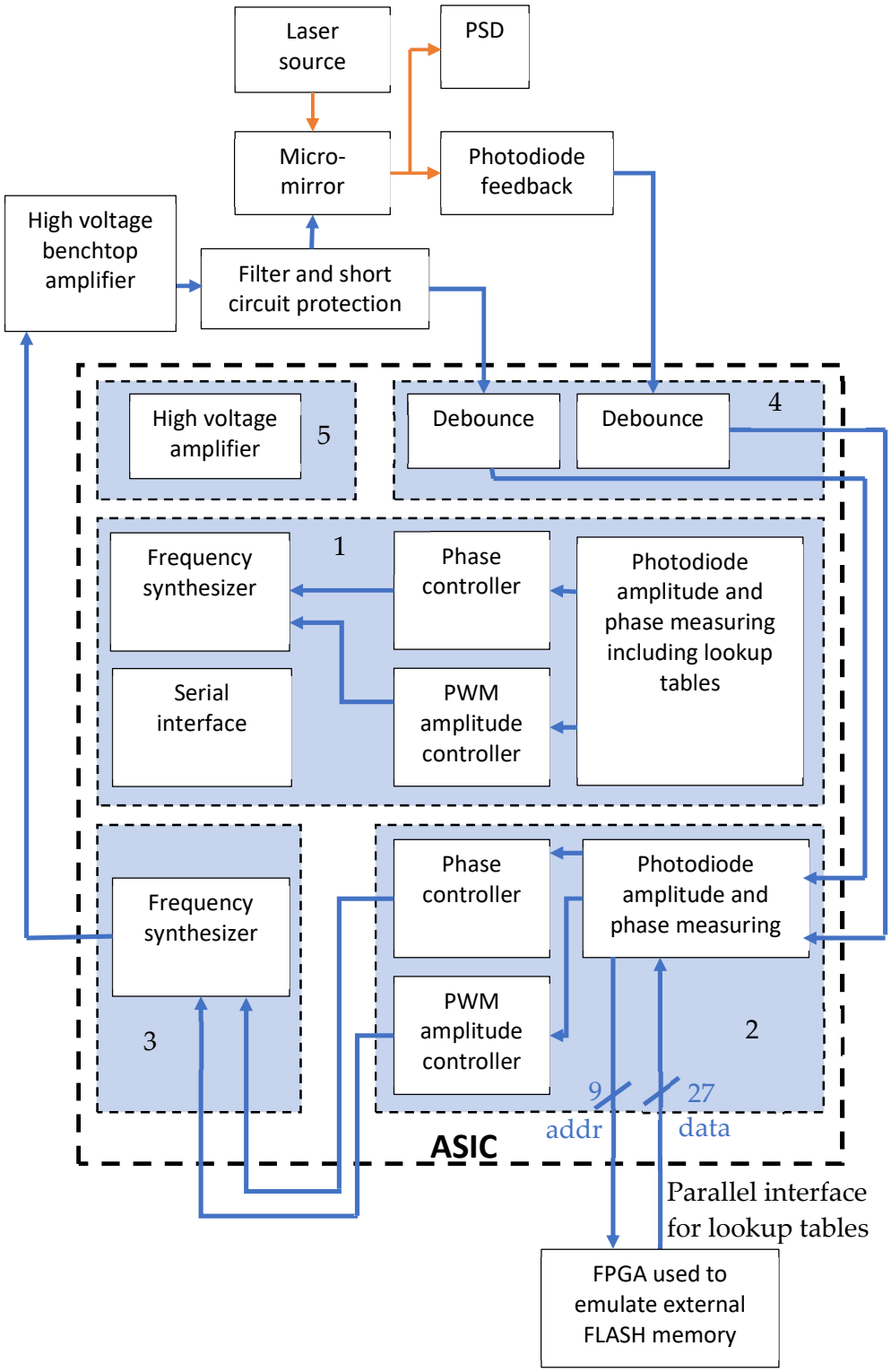

Figure 5-8: Micro-mirror and ASIC block diagram when testing individual blocks of the micro-mirror controller

5.5 High voltage testing of the complete ASIC

During this test, the ASIC high voltage driver was enabled by supplying it with 180 V derived from a benchtop power supply and connecting its input to the output of the embedded digital controller module. A bock diagram of the test setup and ASIC is shown in Figure 5-9. The NBUR pin was connected to the supply voltage which reverse biases diodes D0 and D1 in the circuit shown in Figure 4-12. These reverse bias diodes create and isolated well around the high voltage MOSFETs which allows operation to up to 200 V without leakage to the substate wafer. The drive_limit_low pin as supplied with 6 V and the drive limit_high_pin was supplied with VDD – 6V using reverse biased Zener diodes. These signals are used to limit the gate to drain voltage across the output MOSFETs while ensuring that they are completely turned on when needed.

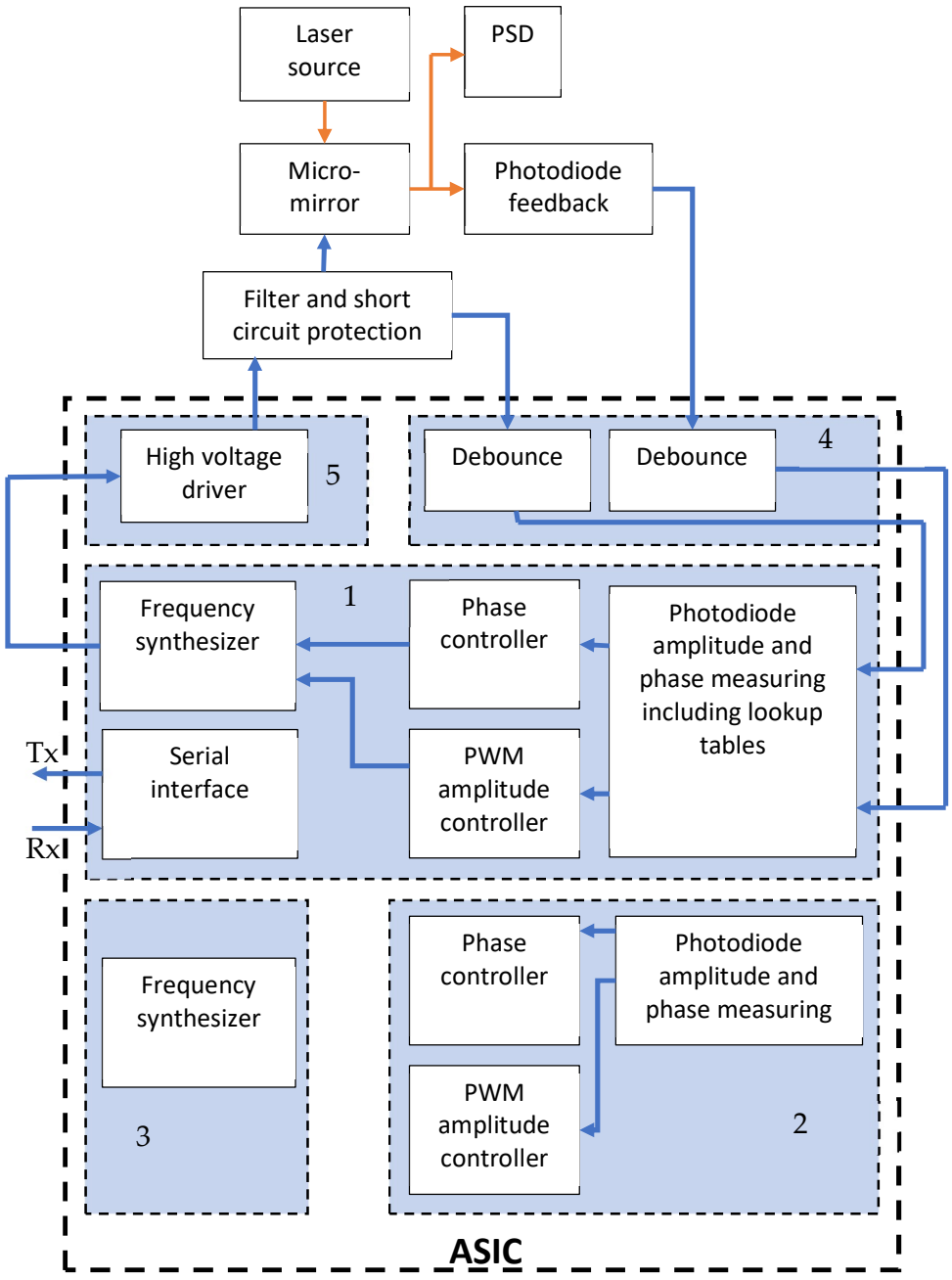

Figure 5-9: Block diagram of the setup used for testing the high voltage driver together with the complete controller.

The corresponding output waveform with the micro-mirror connected is shown in Figure 5-10. A slew rate of 184 V/µs was measured for the rising edge and 512 V/µs for the falling edge. These slew rate values were achieved with a load

capacitance of 145.2 pF consisting of the connecting cables and the micro-mirror itself. The maximum angle of oscillations of the micro-mirror when driven by the controller together with the on-chip high voltage driver was measured using the PSD. The results compared to the previous results using the bench top high voltage amplifier and the ideal angle are shown in Figure 5-11. A good agreement is achieved between the two driving methods.

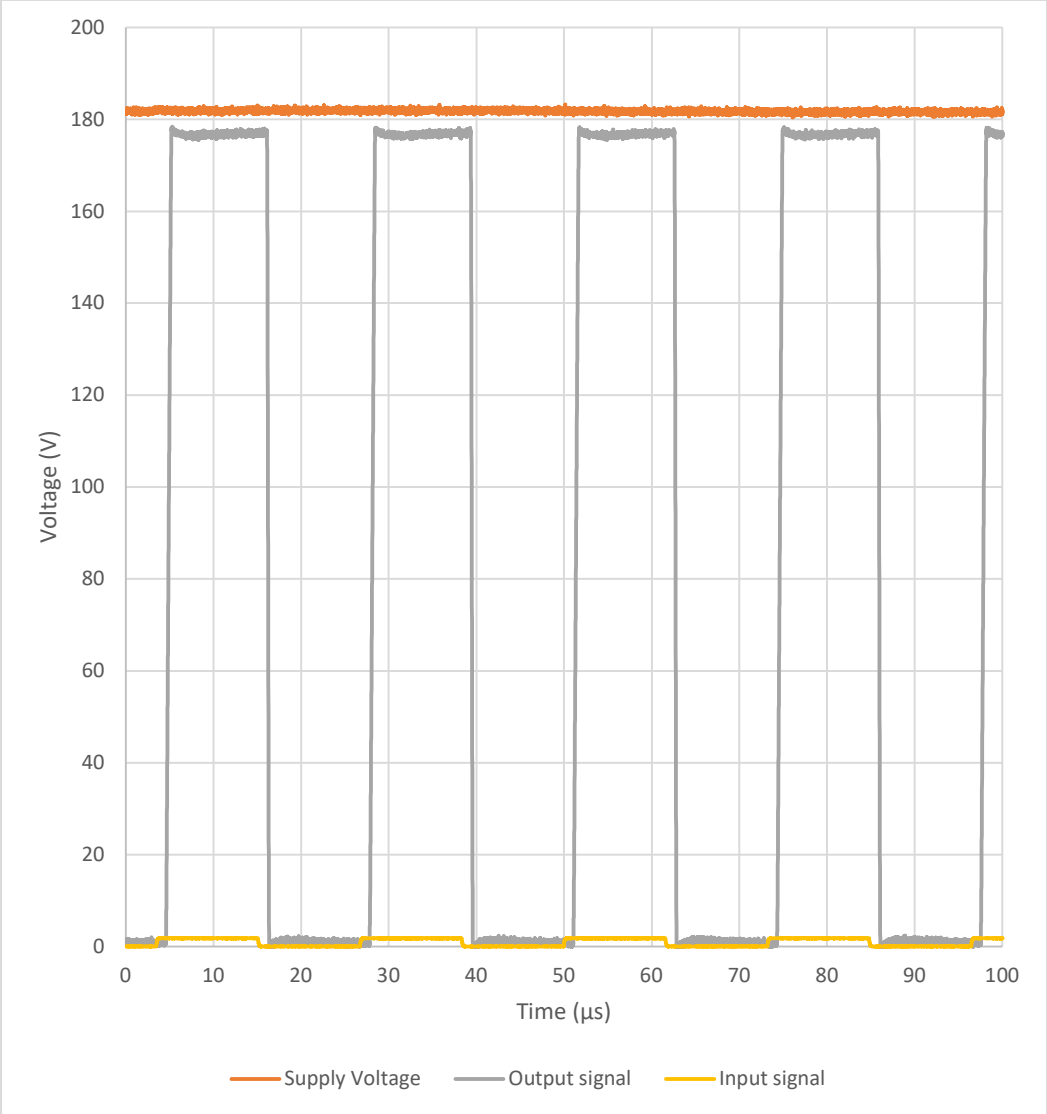

Figure 5-10: High voltage driver input and output signals when operated at 180 V supply

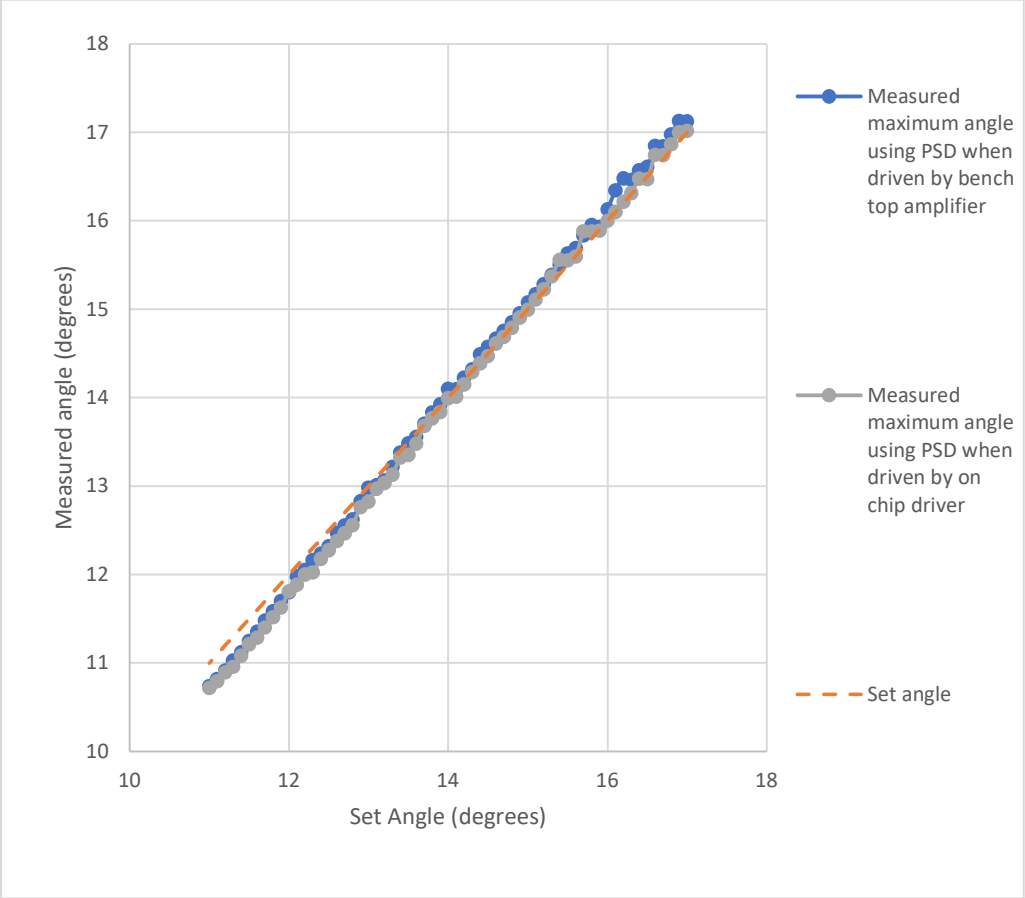

Figure 5-11: Comparing the maximum oscillation angle when the micro-mirror is driven by the bench top high voltage amplifier and the on chip high voltage output.

5.6 Implementation die area

The implementation of the independent amplitude and phase measurement block (Section 4.2.2.2) and drive signal generator block (Section 4.2.2.3) demonstrates that it is possible to implement the controller in a much smaller area than that taken up by the complete controller implementation. This smaller area is achievable by having the lookup tables externally (example on a FLASH IC) and all parameters are fixed at the design stage therefore no serial interface is needed. From this implementation one can deduce that the total area needed by the digital part of the micro-mirror ASIC controller is approximately 1.3 mm^2.

5.7 Conclusion

In this chapter, a novel ASIC that can be used to operate AVC micro-mirrors is evaluated. The evaluation started with successful functional validation of the all-digital closed loop controller implemented here. System level testing was then performed at the optical characterisation facilities available at University of Malta. Closed loop control of the micromirror oscillation amplitude was achieved, thus validating the controller implementation proposed in Chapter 3.

Both testing of the fully integrated controller and of the separate blocks interconnected together off-chip gave results which are equivalent to those observed when an FPGA implementation of the controller was used.

When replacing the external high voltage amplifier with the on-chip high voltage driver, there was no degradation in closed loop amplitude control performance. The ASIC results validate the successful integration of the high voltage driver and the low voltage all-digital controller using a single CMOS technology. The controller RMSE was measured to be 1.58%, which is an improvement in linearity previously publish work [87].

The controller was not tested in a micro-spectrometer because one was not available at the time, and constructing a complete spectrometer was beyond the scope of this research project. However, the results indicate that a positional accuracy of less than 2.8% can be achieved. This can be compared to a commercial micro-spectrometer, such as the C12666MA [88] manufactured by Hamamatsu, which has a spectral resolution of 3.4% of the spectral response range. These findings demonstrate that the proposed controller can position a diffracted light source with greater accuracy than commercial devices.

It is clear that with an implementation that omits duplicate blocks the required die area of the micro-mirror controller can be reduced to much less than what was implemented in this ASIC implementation. Approximately 1.3 mm^2 is

achievable with the mixed-signal process used here, while the use of a dedicated digital CMOS process would reduce the controller area significantly. The limitation of this approach would be the need of a second die for the high voltage driver or an external high voltage driver IC.

These results demonstrate that the controller designed in Chapter 3 and implemented in Chapter 4 is effective in operating the micro-mirror, making it suitable for commercial applications of micro-spectrometers. Specifically, the controller exhibits superior linearity compared to previously published work, and its positional accuracy meets the stringent requirements for high-end micro-spectrometers. Additionally, the results highlight the feasibility of integrating both low-voltage digital logic and high-voltage analogue components on the same die, thereby reducing the overall size of the implementation.

6 Conclusions and future work

This research presents the work carried out on the design of a micro-mirror controller for micro-spectrometer applications. The aim is to design control and drive circuitry for precision control of the micro-mirror amplitude and phase which are needed for such applications. Through the design of innovative controller blocks, a closed loop all-digital controller that can accurately control the phase and amplitude of oscillation of an AVC electrostatic micro-mirror is developed. This controller is simulated and its performance verified using an FPGA and a physical micro-mirror. The feasibility of implementing the controller together with a high voltage waveform generator on a single ASIC manufacturing process is demonstrated. The process used is the XFAB XT-018, a BCD-on-SOI process that integrates both low voltage digital and high voltage analogue on the same die. Measurement using the manufactured ASIC demonstrated the ability of the controller to accurately control the micro-mirror and thus validating its potential use in commercial applications.

6.1 Summary of the Research

The main outcomes of this research are:

- An in-depth analysis was carried out on the energy transfer to an AVC electrostatic resonating micro-mirror for different drive waveforms with the aim of maximising the angle of oscillation. It is demonstrated analytically that a unipolar square wave at double the resonant frequency transfers the highest energy to the micro-mirror and therefore results in the highest amplitude of oscillations. Furthermore, an analysis is carried out on the optimal phase between the applied voltage and the micro-mirror oscillation amplitude. For the unipolar square wave, the

optimal phase is found to be 90°. For a more realistic filtered square wave, the optimal phase is found to be 94°.

- An improvement to a previously published micro-mirror feedback technique is achieved by accurately measuring the phase and amplitude of oscillation of a micro-mirror using the signal from a single photodiode placed in the path of a laser beam reflected off the micro-mirror. This improvement is achieved by relying on timing measurement on rising edges of pulses rather than centre of pulses. An algorithm that uses lookup tables to solve the non-linear equation is implemented on an FPGA and compared to a PSD measurement. With the proposed feedback mechanism using only one photodiode, a higher precision and lower cost micro-spectrometer is possible.
- In an all-digital closed loop micro-mirror oscillations amplitude control logic, the energy transferred to the micro-mirror can be controlled by varying the duty cycle of the drive waveform. This change in duty cycle can be obtained in two ways, by shifting the leading edge while the trailing edge remains stationary with respect to the angle of the oscillation, or the other way round. It is shown here through experimentation, that by shifting the leading edge and keeping the trailing edge stationary, a much more linear transfer function between a duty cycle of 30% to 50% and the oscillation amplitude is obtained. This improved linearity means that a more well-behaved system is obtained and therefore it is easier to control the micro-mirror in closed loop.
- An analytical model of the micro-mirror together with the proposed single photodiode feedback mechanism and a closed loop controller are presented. A phase lock loop is used to control the frequency synthesiser which ensures that the micro-mirror operates at its resonant point. This model is useful as it allows for evaluation of different control parameters before implementing them.

- The innovations presented above were initially implemented entirely as a complete controller on an FPGA in order to validate their performance in regulating the oscillation of a micro-mirror. Since the controller is implemented in all-digital logic, and due to limitations arising from the ratio of the system clock frequency and the output frequency, it is demonstrated that a fractional-N divider is needed. Stable amplitude of oscillations is obtained using two techniques: a Delta-Sigma fractional-N divider and a dithering based fractional-N divider. It is shown that both are equally good at driving the micro-mirror with a stable amplitude of oscillations; however, the dithering technique is simpler to implement and results in a smaller implementation area.

  The implementation in all-digital logic has the advantage that the controller can be implemented on digital only logic which is becoming more and more dense over time. The increased density translates to a smaller die area and therefore a lower cost in high volume applications. Moreover, digital logic is not sensitive to manufacturing variations and therefore guarantees that every device performs equally in controlling the oscillations of a micro-mirror.
- The controller described above, together with a high voltage micro-mirror drive waveform generator are implemented in the XFAB XT018 BCD-on-SOI process. This demonstrates the effectiveness and feasibility of implementing the controller in a commercial situation where high-volume manufacturing is needed. It is demonstrated that the controller without the high voltage driver can be implemented in a total area of less than 1.3 mm^2.

The controller presented in this research was designed in the context of micro-spectrometers; however, it can be applied to other micro-mirror applications. The controller can be easily adapted to be used in applications such as laser

scanners and pico-projectors. These applications would benefit from the improved oscillation amplitude control as better controlled outputs can be achieved.

The proposed controller can also be used to drive resonant micro-mirrors having different types of actuation mechanisms such as piezoelectric and electromagnetic. In such applications the ideal drive waveform and phase may not be the same as in the electrostatic micro-mirror used in this study. Unlike electrostatic micro-mirrors, these actuation types can exert both attractive and repulsive forces and therefore a bipolar waveform will induce a higher energy transfer to the micro-mirror. This can be achieved by replacing the push-pull driver with an H-bridge driver. For applications using electromagnetic micro-mirrors, the high voltage driver needs to be replaced with a high current driver.

6.2 Novel Contribution to the State-of-the-art

Through this research, a better understanding of the energy transfer to an angular vertical combs (AVC) electrostatic micro-mirror for different waveforms is achieved. From this analytical analysis, it is demonstrated that the ideal waveform is a unipolar square wave at double the resonant frequency. The analytical analysis also demonstrates the optimal phase for each actuation waveform and that for the practical waveform, that is a filtered square wave, the optimal phase is 93°.

An improved amplitude and phase measurement technique that uses a single photodiode in the path of a reflected laser beam is developed and demonstrated. This technique requires simpler hardware when compared to a previously published technique that used two photodiodes to compute the amplitude of oscillations [49]. This results in a reduced implementation cost.

An investigation is carried out on the differences in shifting the leading edge or trailing edge when controlling the amplitude of an electrostatic micro-mirror

using a pulse width modulated rectangular wave. Through measurement, it is shown that by keeping the trailing edge fixed at 90°, the micro-mirror has a much more linear response to change in the duty cycle range between 30% and 50%.

The all-digital implementation of the controller requires the use of a fractional-N divider. For this purpose, a technique called dithering described in [60], which was originally developed for communication purposes has been adapted and shown to be effective for stable control of the micro-mirror. This approach is simpler to implement than the alternative delta-sigma fractional-N frequency synthesis technique.

Verification of the controller was carried out via a Simulink model of the controller together with a model of the mechanical parameters of the micro-mirror.

By combining the innovative photodiode feedback mechanism, duty cycle amplitude control, phase locked loop frequency control, and a dithering based fractional-N divider, it is demonstrated that an all-digital micro-mirror controller is feasible. This implementation was first tested on an FPGA platform. It was also demonstrated that the controller can be implemented on an ASIC which integrates also a high voltage micro-mirror driver on the same die.

6.3 Future work

The current implementation focuses on demonstrating the functionality of the micro-mirror controller. This is demonstrated in Section 5.2. In Section 5.6 it is shown that with the current optimisation and using external flash memory, the total area of the controller can be reduced to 1.3 mm^2. Further improvements can be done on minimising the area needed to implement the digital controller.

For example, the code size can be reduced by optimising the bit length of each signal.

Another improvement is to replace the RS232 serial ASCII interface with a more integration friendly solution. This can be achieved by using an industry standard serial protocol such as SPI or I²C and an addressable register protocol for updating the controller parameters and look up tables. These types of protocols are more commonly used for onboard communication and would better suit the final implementation of the micro-mirror controller.

The implemented design integrates the digital and high voltage on the same chip. With digital only logic becoming more compact and cheaper, and considering the simplicity of the high voltage driver used, an alternative approach is to separate the two implementations.

In such approach, the digital logic could be implemented using a lower cost and higher density digital-only process, such as the TSMC 16 nm CMOS Logic [89]. This process is a FinFet solution which offers high density and superior power consumption by operating at a voltage as low as 0.8 V. Moreover, the controller design proposed can be used as an HDL core and be integrated together with the implementation of other components of the final product. For example, in the case of a micro-spectrometer air quality sensor, the digital controller can be implemented together with the digital signal processing block needed to distinguish the sensed gasses.

In the case where the all-digital controller is implemented on digital only process, the high voltage drive circuit can be implemented in two ways: using discrete components on the product PCB; or on a separate die withing the same packaging. The discrete components option can be cheaper to implement due to the simplicity of the circuit; however, the final implementation area on the PCB will be larger. On the other hand, the multi-die chip approach is more

compact; however, the cost can be higher due to the introduced complexity in the packaging process.

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Appendices

Appendix 1: Selected code for implementation of different fractional-N dividers

```
-------------------------------------------------------------------------
-------------------------------------------------------------
-- Generate signal low resolution
-------------------------------------------------------------------------
-------------------------------------------------------------
      process(clk_300,reset)
      begin
            if(rising_edge(clk_300)) then
                  if(reset='1') then
                        counter <= (others => '0');
                        counter_2 <= "00000000000000000000001000";
                        clk1 <= '0';
                        clk2 <= '0';
                  else
                        if(counter > 1045 ) then
                              counter <= (others => '0');
                              clk1 <= not clk1;
                        else
                              counter <= counter +
("00000000000000000001");
                        end if;
                        if(counter_2 > freq ) then
                              counter_2 <= (others => '0');
                              clk2 <= not clk2;
                        else
                              counter_2 <= counter_2 +
("00000000000000000001");
                        end if;
                  end if;
            end if;
      end process;

-------------------------------------------------------------------------
-------------------------------------------------------------
-- generate signal dithering
-------------------------------------------------------------------------
-------------------------------------------------------------
      process (clk_100,reset)
      begin
            if(reset='1') then
                  accum <= 0;

            elsif(rising_edge(clk_100)) then
                  if (accum >= target) then
                        clk3 <= not clk3;
                        accum <= accum - target+step;
                  else
                        accum <= accum + step;
                  end if;
            end if;
```

```
	end process;
-------------------------------------------------------------------
-------------------------------------------------------------
-- generate signal high resolution fractional N
-------------------------------------------------------------------
-------------------------------------------------------------
	process (clk_100,reset)
	begin
		if(reset='1') then
			seq_ctr <= 0;
		elsif(rising_edge(clk_100)) then
			if (term_count = '1') then
				if (seq_ctr = 0) then
					seq_ctr <= C-1;
				else
					seq_ctr <= seq_ctr - 1;
				end if;
			end if;
		end if;
	end process;
	mux_select <= '1' when (seq_ctr < B_count) else '0';
	dual_mod_load <= (N) when (mux_select = '1') else (N-1);

	process (clk_100,reset)
	begin
		if(reset='1') then
			dual_mod_ctr <= 0;
		elsif(rising_edge(clk_100)) then
			if (term_count = '1') then
				dual_mod_ctr <= dual_mod_load;
				clk4 <= not clk4;
			else
				dual_mod_ctr <= dual_mod_ctr - 1;
			end if;
		end if;
	end process;

	-- Detect the terminal count condition
	term_count <= '1' when (dual_mod_ctr = 0) else '0';

-------------------------------------------------------------------
-------------------------------------------------------------
-- generate signal high resolution fractional N Sigma Delta
-------------------------------------------------------------------
-------------------------------------------------------------
	process (clk_100,reset)
	begin
		if(rising_edge(clk_100)) then
			if(reset='1') then
					G1 <= 0;
					G3 <= 0;
					G2 <= 0;
					Y  <= 0;
			else
				if (ctr_SD = 0) then

					G1 <= B_count - Y;
					G3 <= G2;
					G2 <= G1 + G3;

					if G3 >= 0 then		--Quantizer
```

```
                        Y <= 1000;
                    else
                        y <= 0;
                    end if;

                end if;
            end if;
        end if;
end process;

mux_select_2 <= '1' when (Y = 1000) else '0';
dual_mod_load_2 <= (N) when (mux_select_2 = '1') else (N-1);

process (clk_100,reset)
begin
        if(reset='1') then
            ctr_SD <= 0;
        elsif(rising_edge(clk_100)) then
            if (ctr_SD = 0) then
                ctr_SD <= dual_mod_load_2;
                clk5 <= not clk5;
            else
                ctr_SD <= ctr_SD - 1;
            end if;
        end if;
end process;
```

Appendix 2: Selected code for implementation of controller including amplitude and phase closed loop control

```
-----------------------------------------------------------------------
-----------------------------------------------------------
--Read photodiode and voltage
-----------------------------------------------------------------------
-----------------------------------------------------------
      process (clk_main,reset)
      begin
            if(reset='1') then
                  counter_3 <= 0;
            elsif(rising_edge(clk_main)) then
                  counter_3  <= counter_3 + 1;
                  photodiode_old <= photodiode;
                  photodiode_old_old <= photodiode_old;
                  voltage_old <= voltage;
                  voltage_old_2 <= voltage_old;

                  if ( voltage_old = '0' and voltage_old_2 = '1')then

                        if phase_lock_mode = '0' then       -- lock
to phase error of 0
                              if (phase_error > 0) then
                                    e <= "01";
                              elsif (phase_error < 0) then
                                    e <= "10";
                              else
                                    e <= "00";
                              end if;
                        else
      --lock to phase of 90
                              if (phase > (T1_T2/4)) then
                                    e <= "01";
                              elsif (phase < (T1_T2/4)) then
                                    e <= "10";
                              else
                                    e <= "00";
                              end if;
                        end if;

                        if (amplitude > amplitude_set) then
                              e_duty <= "01";
                        elsif (amplitude < amplitude_set)  then
                              e_duty <= "10";
                        else
                              e_duty <= "00";
                        end if;

                  end if;

                  if ( voltage_old = '1' and voltage_old_2 = '0')then
                        counter_3_voltage <= counter_3;
                        voltage_period <= counter_3 -
counter_3_voltage;
                  end if;

                  if ( voltage_old = '0' and voltage_old_2 = '1')then
```

```
                        voltage_high <= counter_3 -
counter_3_voltage;
                  end if;

                  if (counter_3 - counter_3_T) > voltage_period +
(voltage_period/2) then
                        oscillating <= '0';
                  end if;

                  if oscillating = '0' then
                        phase <= 0;
                        phase_error <= 0;
                        amplitude <= 0;
                  else
                        amplitude <= lookup_amplitude;
                  end if;
                  if (photodiode_old = '1' and photodiode_old_old =
'0')then    --Detect rising edge in photodiode pulse
                        if (counter_3 - counter_3_T) >
(voltage_period + (voltage_period/2)) then --Check if micro-mirror
oscillating by checking is longer than voltage periode *1.5
                              oscillating <= '0';                 --
if not oscillating reset signal
                              phase <= 0;
                              phase_error <= 0;
                              amplitude <= 0;
                        else
                              oscillating <= '1';
                              if (counter_3 - counter_3_T <
(voltage_period)) then --identify if measuring T1 of T2 since T1 is
shorter than voltage period and T2 is longer
                                    T1 <= counter_3 - counter_3_T;
                                    T1_T2 <= counter_3 - counter_3_T
+ T2;
                              else
                                    T2 <= counter_3 - counter_3_T;
                                    T1_T2 <= counter_3 - counter_3_T
+ T1;
                                    phase <= ((counter_3 -
counter_3_voltage)- lookup_phase);
                                    phase_error <= (((counter_3 -
counter_3_voltage)- lookup_phase) - voltage_high);
                              end if;
                        end if;
                        counter_3_T <= counter_3;
                  end if;
            end if;
      end process;
-------------------------------------------------------------------
-------------------------------------------------------------
--Lookup table
-------------------------------------------------------------------
-------------------------------------------------------------
      addr_3 <= ( ( T1 * 2048 ) / ( T1 + (T2 ) ) ) - 512;
      lookup_amplitude <=  angle_look_up (addr_3);
      lookup_phase <= phase_look_up (addr_3) * ( T1 + T2 )/(2**16) ;

-------------------------------------------------------------------
-------------------------------------------------------------
-- generate signal high resolution dithering and duty cycle control
```

```
-----------------------------------------------------------------------
-----------------------------------------------------------------
      process (clk_main,reset)
      begin
            if(reset='1') then
                  accum <= 0;

            elsif(rising_edge(clk_main)) then

                  counter_timer <= counter_timer + 1;

                  if counter_timer - target_counter_timer >=
(f_in/20000) then       --PLL loop update
                        target_counter_timer <= counter_timer;

                        if PLL_enable = '0' then
                                          --disable frequency control
                              target <= target_input;

                        elsif oscillating = '0' then
                  -- if not oscillating sweep
                              if target < target_upper_limit then
            --frequency got too high
                                    direction <= '1';
                  --increment target i.e. reduce frequency
                              end if;
                              if target > target_lower_limit then
            --frequency got too loo
                                    direction <= '0';
                  --decrement target i.e. increase frequency
                              end if;
                              if direction = '0' then
                                    target <= target-1;
                              else
                                    target <= target+1;
                              end if;

                        elsif e = "01" then
                              --use error 'e' to adjust output
frequency
                              target <= target + 1;
                        elsif e = "10" then
                              target <= target - 1;
                        end if;
                  end if;

                  if counter_timer - duty_cycle_counter_timer >=
(f_in/200) then         --amplitude control loop update
                        duty_cycle_counter_timer <= counter_timer;

                        if amplitude_control_enable = '0' then
                                                --disable
amplitude control
                              duty_cycle <= duty_cycle_input;
                        else
                              if (e_duty = "01") and (duty_cycle >
integer((2**10)*0.1) ) then --use error 'e_duty' to adjust amplitude
                                    duty_cycle <= duty_cycle - 1;
                              end if;
                              if (e_duty = "10") and (duty_cycle <
integer((2**10)*0.5) ) then
```

```
                                    duty_cycle <= duty_cycle + 1;
                              end if;
                        end if;
                  end if;

                  if (accum >= target) then
                              --dithering signal generator
                        clk_dethering <= '1';
                        accum <= accum - target+step;
                  elsif (accum >=((target*duty_cycle)/2**10)) then
                        clk_dethering <= '0';
                        accum <= accum + step;
                  else
                        clk_dethering <= '1';
                        accum <= accum + step;
                  end if;
            end if;
      end process;
-------------------------------------------------------------------------
-------------------------------------------------------------
--Read data from serial
-------------------------------------------------------------------------
-------------------------------------------------------------
      process (clk_main,reset)
      begin
            if(reset='1') then

                  angle_look_up <= (840 ,840 ,841 ,842 ,843 ,844 ,845
,846 ,847 ,847 ,848 ,849 ,850 ,851 ,852 ,853 ,854 ,855 ,856 ,857 ,858
,859 ,860 ,861 ,862 ,863 ,864 ,865 ,866 ,867 ,868 ,869 ,870 ,871 ,872
,873 ,874 ,876 ,877 ,878 ,879 ,880 ,881 ,882 ,884 ,885 ,886 ,887 ,888
,889 ,891 ,892 ,893 ,894 ,896 ,897 ,898 ,899 ,901 ,902 ,903 ,905 ,906
,907 ,909 ,910 ,911 ,913 ,914 ,915 ,917 ,918 ,920 ,921 ,922 ,924 ,925
,927 ,928 ,930 ,931 ,933 ,934 ,936 ,937 ,939 ,940 ,942 ,943 ,945 ,947
,948 ,950 ,951 ,953 ,955 ,956 ,958 ,960 ,961 ,963 ,965 ,966 ,968 ,970
,972 ,973 ,975 ,977 ,979 ,981 ,982 ,984 ,986 ,988 ,990 ,992 ,994 ,995
,997 ,999 ,1001 ,1003 ,1005 ,1007 ,1009 ,1011 ,1013 ,1015 ,1017 ,1019
,1021 ,1023 ,1025 ,1028 ,1030 ,1032 ,1034 ,1036 ,1038 ,1040 ,1043
,1045 ,1047 ,1049 ,1052 ,1054 ,1056 ,1059 ,1061 ,1063 ,1066 ,1068
,1070 ,1073 ,1075 ,1078 ,1080 ,1082 ,1085 ,1087 ,1090 ,1092 ,1095
,1098 ,1100 ,1103 ,1105 ,1108 ,1111 ,1113 ,1116 ,1119 ,1121 ,1124
,1127 ,1130 ,1133 ,1135 ,1138 ,1141 ,1144 ,1147 ,1150 ,1153 ,1156
,1159 ,1162 ,1165 ,1168 ,1171 ,1174 ,1177 ,1180 ,1183 ,1186 ,1190
,1193 ,1196 ,1199 ,1203 ,1206 ,1209 ,1213 ,1216 ,1219 ,1223 ,1226
,1230 ,1233 ,1237 ,1240 ,1244 ,1248 ,1251 ,1255 ,1259 ,1262 ,1266
,1270 ,1274 ,1277 ,1281 ,1285 ,1289 ,1293 ,1297 ,1301 ,1305 ,1309
,1313 ,1317 ,1321 ,1326 ,1330 ,1334 ,1338 ,1343 ,1347 ,1351 ,1356
,1360 ,1365 ,1369 ,1374 ,1379 ,1383 ,1388 ,1393 ,1397 ,1402 ,1407
,1412 ,1417 ,1422 ,1427 ,1432 ,1437 ,1442 ,1447 ,1452 ,1458 ,1463
,1468 ,1474 ,1479 ,1484 ,1490 ,1496 ,1501 ,1507 ,1513 ,1518 ,1524
,1530 ,1536 ,1542 ,1548 ,1554 ,1560 ,1566 ,1572 ,1579 ,1585 ,1592
,1598 ,1604 ,1611 ,1618 ,1624 ,1631 ,1638 ,1645 ,1652 ,1659 ,1666
,1673 ,1680 ,1688 ,1695 ,1703 ,1710 ,1718 ,1725 ,1733 ,1741 ,1749
,1757 ,1765 ,1773 ,1781 ,1789 ,1798 ,1806 ,1815 ,1823 ,1832 ,1841
,1850 ,1859 ,1868 ,1877 ,1886 ,1896 ,1905 ,1915 ,1925 ,1935 ,1944
,1954 ,1965 ,1975 ,1985 ,1996 ,2006 ,2017 ,2028 ,2039 ,2050 ,2061
,2073 ,2084 ,2096 ,2107 ,2119 ,2131 ,2144 ,2156 ,2168 ,2181 ,2194
,2207 ,2220 ,2233 ,2247 ,2260 ,2274 ,2288 ,2302 ,2317 ,2331 ,2346
,2361 ,2376 ,2391 ,2407 ,2423 ,2438 ,2455 ,2471 ,2488 ,2505 ,2522
,2539 ,2557 ,2574 ,2592 ,2611 ,2629 ,2648 ,2668 ,2687 ,2707 ,2727
,2747 ,2768 ,2789 ,2810 ,2832 ,2854 ,2876 ,2899 ,2922 ,2946 ,2969
```

```
,2994 ,3018 ,3043 ,3069 ,3095 ,3121 ,3148 ,3176 ,3203 ,3232 ,3260
,3290 ,3320 ,3350 ,3381 ,3413 ,3445 ,3478 ,3511 ,3545 ,3580 ,3615
,3651 ,3688 ,3726 ,3764 ,3803 ,3843 ,3884 ,3926 ,3968 ,4012 ,4056
,4102 ,4148 ,4196 ,4244 ,4294 ,4345 ,4397 ,4451 ,4505 ,4561 ,4619
,4677 ,4738 ,4799 ,4863 ,4928 ,4995 ,5063 ,5134 ,5206 ,5280 ,5357
,5435 ,5516 ,5599 ,5685 ,5773 ,5864 ,5957 ,6054 ,6153 ,6256 ,6362
,6471 ,6584 ,6701 ,6821 ,6946 ,7075 ,7209 ,7347 ,7490 ,7639 ,7793
,7953 ,8119 ,8291 ,8470 ,8655 ,8849 ,9050 ,9259 ,9476 ,9703 ,9939
,10185 ,10441 ,10709 ,10987 ,11278 ,11581 ,11898 ,12228 ,12572 ,12931
,13306 ,13696 ,14102 ,14526 ,14966 ,15423 ,15897 ,16389 ,16898 ,17423
,17965 ,18522 ,19094 ,19679 ,20276 ,20883 ,21499 ,22121 ,22748) ;
                phase_look_up <= (3692 ,3688 ,3684 ,3680 ,3676
,3672 ,3668 ,3664 ,3660 ,3656 ,3652 ,3648 ,3644 ,3640 ,3635 ,3631
,3627 ,3623 ,3619 ,3614 ,3610 ,3606 ,3601 ,3597 ,3593 ,3588 ,3584
,3579 ,3575 ,3570 ,3566 ,3561 ,3557 ,3552 ,3548 ,3543 ,3538 ,3534
,3529 ,3524 ,3519 ,3515 ,3510 ,3505 ,3500 ,3495 ,3491 ,3486 ,3481
,3476 ,3471 ,3466 ,3461 ,3456 ,3451 ,3446 ,3441 ,3436 ,3431 ,3426
,3421 ,3415 ,3410 ,3405 ,3400 ,3395 ,3389 ,3384 ,3379 ,3374 ,3368
,3363 ,3358 ,3352 ,3347 ,3341 ,3336 ,3331 ,3325 ,3320 ,3314 ,3309
,3303 ,3298 ,3292 ,3286 ,3281 ,3275 ,3270 ,3264 ,3258 ,3253 ,3247
,3241 ,3235 ,3230 ,3224 ,3218 ,3212 ,3207 ,3201 ,3195 ,3189 ,3183
,3177 ,3171 ,3165 ,3159 ,3154 ,3148 ,3142 ,3136 ,3130 ,3123 ,3117
,3111 ,3105 ,3099 ,3093 ,3087 ,3081 ,3075 ,3068 ,3062 ,3056 ,3050
,3044 ,3037 ,3031 ,3025 ,3019 ,3012 ,3006 ,3000 ,2993 ,2987 ,2981
,2974 ,2968 ,2961 ,2955 ,2948 ,2942 ,2936 ,2929 ,2923 ,2916 ,2910
,2903 ,2896 ,2890 ,2883 ,2877 ,2870 ,2864 ,2857 ,2850 ,2844 ,2837
,2830 ,2824 ,2817 ,2810 ,2803 ,2797 ,2790 ,2783 ,2776 ,2770 ,2763
,2756 ,2749 ,2742 ,2736 ,2729 ,2722 ,2715 ,2708 ,2701 ,2694 ,2687
,2680 ,2673 ,2666 ,2659 ,2652 ,2645 ,2638 ,2631 ,2624 ,2617 ,2610
,2603 ,2596 ,2589 ,2582 ,2575 ,2568 ,2561 ,2553 ,2546 ,2539 ,2532
,2525 ,2518 ,2510 ,2503 ,2496 ,2489 ,2481 ,2474 ,2467 ,2460 ,2452
,2445 ,2438 ,2431 ,2423 ,2416 ,2409 ,2401 ,2394 ,2386 ,2379 ,2372
,2364 ,2357 ,2349 ,2342 ,2335 ,2327 ,2320 ,2312 ,2305 ,2297 ,2290
,2282 ,2275 ,2267 ,2260 ,2252 ,2245 ,2237 ,2230 ,2222 ,2214 ,2207
,2199 ,2192 ,2184 ,2176 ,2169 ,2161 ,2153 ,2146 ,2138 ,2130 ,2123
,2115 ,2107 ,2100 ,2092 ,2084 ,2077 ,2069 ,2061 ,2053 ,2046 ,2038
,2030 ,2022 ,2015 ,2007 ,1999 ,1991 ,1983 ,1975 ,1968 ,1960 ,1952
,1944 ,1936 ,1928 ,1921 ,1913 ,1905 ,1897 ,1889 ,1881 ,1873 ,1865
,1857 ,1849 ,1841 ,1833 ,1826 ,1818 ,1810 ,1802 ,1794 ,1786 ,1778
,1770 ,1762 ,1754 ,1746 ,1738 ,1730 ,1722 ,1714 ,1705 ,1697 ,1689
,1681 ,1673 ,1665 ,1657 ,1649 ,1641 ,1633 ,1625 ,1617 ,1608 ,1600
,1592 ,1584 ,1576 ,1568 ,1560 ,1551 ,1543 ,1535 ,1527 ,1519 ,1511
,1502 ,1494 ,1486 ,1478 ,1470 ,1461 ,1453 ,1445 ,1437 ,1428 ,1420
,1412 ,1404 ,1395 ,1387 ,1379 ,1371 ,1362 ,1354 ,1346 ,1338 ,1329
,1321 ,1313 ,1304 ,1296 ,1288 ,1279 ,1271 ,1263 ,1254 ,1246 ,1238
,1229 ,1221 ,1213 ,1204 ,1196 ,1188 ,1179 ,1171 ,1163 ,1154 ,1146
,1137 ,1129 ,1121 ,1112 ,1104 ,1095 ,1087 ,1079 ,1070 ,1062 ,1053
,1045 ,1037 ,1028 ,1020 ,1011 ,1003 ,994 ,986 ,977 ,969 ,961 ,952
,944 ,935 ,927 ,918 ,910 ,901 ,893 ,884 ,876 ,867 ,859 ,850 ,842 ,833
,825 ,816 ,808 ,799 ,791 ,782 ,774 ,765 ,757 ,748 ,740 ,731 ,723 ,714
,705 ,697 ,688 ,680 ,671 ,663 ,654 ,646 ,637 ,628 ,620 ,611 ,603 ,594
,586 ,577 ,569 ,560 ,551 ,543 ,534 ,526 ,517 ,508 ,500 ,491 ,483 ,474
,465 ,457 ,448 ,440 ,431 ,423 ,414 ,405 ,397 ,388 ,379 ,371 ,362 ,354
,345 ,336 ,328 ,319 ,311 ,302 ,293 ,285 ,276 ,268 ,259 ,250 ,242 ,233
,224 ,216 ,207 ,199 ,190 ,181 ,173 ,164 ,155 ,147 ,138 ,129 ,121 ,112
,104 ,95 ,86 ,78 ,69 ,60 ,52 ,43 ,35 ,26 ,17 ,9 );

                target_input <= step*f_in/(f_out);
                duty_cycle_input <= 512;
            elsif(rising_edge(clk_main)) then
```

```
                    if (data_vld = '1' and data_vld_old = '0')then
                          case state is
                          when idle =>
                                freq_ready <= '0';
                                read_angle_enable <= '0';
                                read_phase_enable <= '0';
                                serial_num <= 0;
                                case data_out is
                                when "01110010" =>      state <= rst;
                                --r   reset
                                when "01110011" =>      state <= amp;
                                --s   set amplitude
                                when "01100101" =>      state <=
inc_duty;                       --e   increment duty
                                when "01100110" =>      state <=
dec_duty;                       --f   decrement duty
                                when "01100111" =>      state <= inc_t;
                                --g   increment_f
                                when "01101000" =>      state <= dec_t;
                                --h   decrement_f
                                when "01101100" =>      state <=
target_upper;                   --l   target_upper
                                when "01101101" =>      state <=
target_lower;                   --m   target_lower
                                when "01110000" =>      state <=
angle_addr;                     --p   angle address
                                when "01110001" =>      state <=
angle_data;                     --q   angle data
                                when "01101110" =>      state <=
read_angle_addr;        --n     read_angle address
                                when "01110101" =>      state <=
phase_addr;                     --u   phase address
                                when "01110110" =>      state <=
phase_data;                     --v   phase_data
                                when "01110111" =>      state <=
read_phase_addr;        --w     read_phase_address
                                when "01100011" =>      state <= reply;
                                --c   reply
                                when others =>          state <= idle;
                          end case;

                          when rst =>


                                                        --reset
                                case data_out is
                                when "00001010" =>      state <= rst;
                  --newline

                  duty_cycle_input <= 512;

            target_input <= step*f_in/(f_out);
--
                  target_update <= '1';
                                when others =>          state <= idle;
                          end case;

                          when amp =>


                                                        --set amplitude
```

```
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      amplitude_set <=  serial_num;
                              when others =>          state <= idle;
                        end case;

                        when inc_duty =>


                                                --increment duty
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

                  if ((duty_cycle_input + serial_num) > 923) then

                        duty_cycle_input <= 923;

                  else

                        duty_cycle_input  <= duty_cycle_input +
serial_num;

                  end if;
                              when others =>          state <= idle;
                        end case;

                        when dec_duty  =>


                                                --decrement duty
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

                  if ((duty_cycle_input - serial_num) < 100) then

                        duty_cycle_input <= 100;

                  else
```

```
                        duty_cycle_input  <= duty_cycle_input -
serial_num;

                  end if;
                              when others =>          state <= idle;
                        end case;

                        when inc_t =>


                                                      --increment_f
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      target_input <= target_input + serial_num;
--
            target_update <= '1';
                              when others =>          state <= idle;
                        end case;

                        when dec_t =>


                                                      --decrement_f
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      target_input <= target_input - serial_num;
--
            target_update <= '1';
                              when others =>          state <= idle;
                        end case;

                        when target_upper =>


                                          --target_upper
                        case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline
```

```
      target_upper_limit <= serial_num;
                              when others =>          state <= idle;
                        end case;

                        when target_lower =>


                                                --target_lower
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      target_lower_limit <= serial_num;
                              when others =>          state <= idle;
                        end case;

                        when angle_addr =>


                                                --angle address
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      angle_address <= serial_num;
                              when others =>          state <= idle;
                        end case;

                        when angle_data =>


                                                --angle data
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      angle_look_up(angle_address) <=  serial_num;
                              when others =>          state <= idle;
                        end case;

                        when read_angle_addr =>
```

```
                                        --read_angle address
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      read_angle  <= serial_num;

      read_angle_enable <= '1';
                              when others =>          state <= idle;
                        end case;

                        when phase_addr =>


                                        --phase_address
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      phase_address <= serial_num;
                              when others =>          state <= idle;
                        end case;

                        when phase_data =>


                                        --phase_data
                              case data_out is
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      phase_look_up(phase_address) <=  serial_num;
                              when others =>          state <= idle;
                        end case;

                        when read_phase_addr =>


                                        --read_phase_address
                              case data_out is
```

```
                              when "00110000" | "00110001" |
"00110010" | "00110011" | "00110100" | "00110101" | "00110110" |
"00110111" | "00111000" | "00111001" =>

      serial_num <= 10 * serial_num + to_integer(unsigned(data_out(3
downto 0)));
                              when "00001010" =>      state <= idle;
            --newline

      read_phase  <=phase_look_up(serial_num);

      read_phase_enable <= '1';
                              when others =>          state <= idle;
                        end case;

                        when reply =>


                                                      --reply
                              case data_out is
                              when "00001010" =>      state <= idle;
            --newline

      freq_ready <= '1';
                              when others =>          state <= idle;
                        end case;

                        when others =>
                              state <= idle;
                        end case;
                  else
                        freq_ready <= '0';
                        read_angle_enable <= '0';
                        read_phase_enable <= '0';
                  end if;
                  data_vld_old <= data_vld;
            end if;
      end process;

-------------------------------------------------------------------
-------------------------------------------------------------
--Send data over serial
-------------------------------------------------------------------
-------------------------------------------------------------
      process (clk_main,reset)
      begin
            if(reset='1') then

            elsif(rising_edge(clk_main)) then
                  if (send_num = "00000") then
                        if (freq_ready = '1' )then
                              BCD_DATA_IN <= std_logic_vector(
to_unsigned( voltage_period, 24));
                  --1   voltage_period
                              send_num <= "00001";
                              send_bcd <= "00000";
                        end if;
                        if (read_angle_enable = '1' )then
                              BCD_DATA_IN <= std_logic_vector(
to_unsigned( angle_look_up(read_angle), 24));
```

```
                              send_num <= "10000";                --
this should reply with just one number currently set in BCD_DATA_IN
                              send_bcd <= "00000";
                        end if;
                        if (read_phase_enable = '1' )then
                              BCD_DATA_IN <=std_logic_vector(
to_unsigned( phase_look_up(read_phase), 24))  ;
                              send_num <= "10000";                --
this should reply with just one number currently set in BCD_DATA_IN
                              send_bcd <= "00000";
                        end if;
                        data_send <= '0';


                  elsif (send_num <= "10000" and busy = '0' and
data_send = '0') then ------------------------------------------------
-
                        send_bcd <= send_bcd + "00001";
                        data_send <= '1';
                        if (send_bcd = "00000") then
      --Start and send sign
                              data_send <= '1';
                              if (send_sign = '1') then
                                    data_in <= "00101101" ;
                              else
                                    data_in <= "00000000" ;
                              end if;
                        elsif (send_bcd = "00001") then
      --Send 1/8
                              data_in <= "0011" & BCD_DATA_OUT ( 31
downto 28) ;
                        elsif (send_bcd = "00010") then
      --Send 2/8
                              data_in <= "0011" & BCD_DATA_OUT ( 27
downto 24) ;
                        elsif (send_bcd = "00011") then
      --Send 3/8
                              data_in <= "0011" & BCD_DATA_OUT ( 23
downto 20) ;
                        elsif (send_bcd = "00100") then
      --Send 4/8
                              data_in <= "0011" & BCD_DATA_OUT ( 19
downto 16) ;
                        elsif (send_bcd = "00101") then
      --Send 5/8
                              data_in <= "0011" & BCD_DATA_OUT ( 15
downto 12) ;
                        elsif (send_bcd = "00110") then
      --Send 6/8
                              data_in <= "0011" & BCD_DATA_OUT ( 11
downto 8) ;
                        elsif (send_bcd = "00111") then
      --Send 7/8
                              data_in <= "0011" & BCD_DATA_OUT ( 7
downto 4) ;
                        elsif (send_bcd = "01000") then
      --Send 8/8
                              data_in <= "0011" & BCD_DATA_OUT ( 3
downto 0) ;
                        elsif (send_bcd = "01001") then
      --Send new line and pre-load bcd data in
```

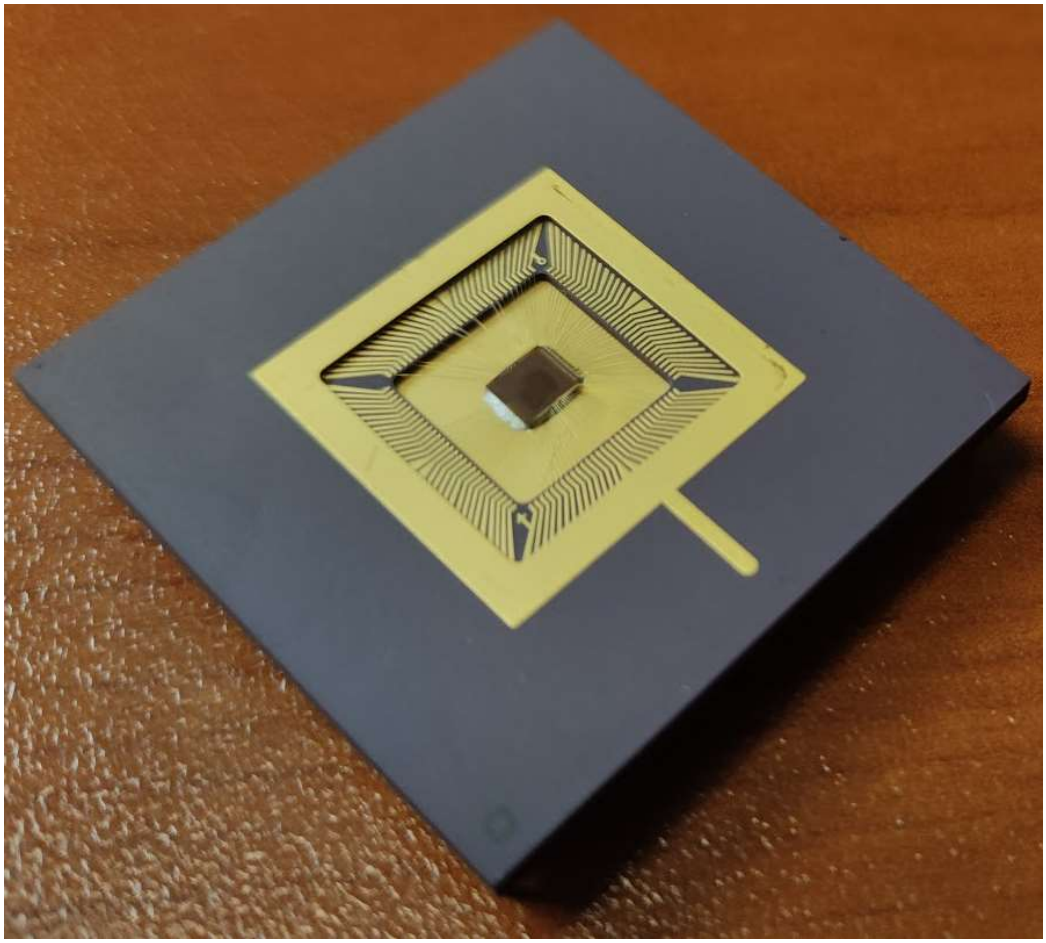
```
                        data_in <= "00100000";
            --space
                        send_bcd <= "00000";
                        send_num <= send_num +"00001";
                        case send_num is
                              when "00001"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
duty_cycle, 24));             --2   next number
                              when "00010"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned( T2,
24));                               --3
                              when "00011"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
voltage_period, 24));         --4
                              when "00100"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
amplitude, 24));              --5
                              when "00101"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned( phase,
24));                               --6
                              when "00110"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned( T1,
24));                               --7
                              when "00111"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned( T1_T2,
24));                               --8
                              when "01000"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned( T1,
24));                               --9
                              when "01001"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
target_upper_limit, 24));     --10
                              when "01010"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
target_lower_limit, 24));     --11
                              when "01011"      => if
(phase_error < 0 ) then

                  --12

            send_sign<='1';

            BCD_DATA_IN <= std_logic_vector( to_unsigned( -
phase_error, 24));

      else

            send_sign<='0';

            BCD_DATA_IN <= std_logic_vector( to_unsigned(
phase_error, 24));

      end if;
                              when "01100"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
voltage_high, 24));           --13
                              when "01101"      => if
(counter_3 < 0 ) then

                  --14
```

```
            send_sign<='1';

            BCD_DATA_IN <= std_logic_vector( to_unsigned( -counter_3,
24));

      else

            send_sign<='0';

            BCD_DATA_IN <= std_logic_vector( to_unsigned( counter_3,
24));

      end if;
                                    when "01110"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned( addr_3,
24));                         --15
                                    when "01111"      =>
send_sign<='0'; BCD_DATA_IN <= std_logic_vector( to_unsigned(
lookup_phase, 24));           --16
                                    when "10000"      =>
send_sign<='0'; BCD_DATA_IN <= "000000000000000000000000"; data_in <=
"00001010"; send_num <= "00000";    --new line
                                    when others =>  BCD_DATA_IN <=
"000000000000000000000000";
                              end case;

                        end if;
                  else
                        --send_num <= "00000";
                        data_send <= '0';
                  end if;
            end if;
      end process;
```

Appendix 3: Debounce logic VHDL code

```
entity debounce is
    Port ( clk : in  STD_LOGIC;
           reset : in  STD_LOGIC;
           signal_in : in  STD_LOGIC;
           signal_out : out  STD_LOGIC);
end debounce;

architecture Behavioral of debounce is

signal signal_in_1 : std_logic;
signal signal_in_2 : std_logic;
signal count : STD_LOGIC_VECTOR(2 downto 0) := "000";

begin

    process (clk,reset)
    begin
        if(reset='1') then
            count <= "000";
            signal_in_1 <= signal_in;
            signal_in_2 <= signal_in_1;
        elsif(rising_edge(clk)) then

            signal_in_1 <= signal_in;
            signal_in_2 <= signal_in_1;

            If(((signal_in_1 xor signal_in_2) = '1') and (count =
"000")) THEN
                signal_out <= signal_in_1;
                count <= "001";
            ELSIF(count > "000") THEN --stable input time is not yet
met
                count <= count + "001";
            end if;

        end if;
    end process;
end Behavioral;
```

Appendix 4: Photos of manufactured IC.



Appendix 5: Photos and details of the PCBs used for testing.

Dimensions	**10cm x 10 cm**
Material	1.6mm 2-layer FR4 PCB
Interface	8 SMA connectors and pin headers
Input power	3.3V to 5V DC

Dimensions	**12cm x 14cm**
Material	1.6mm 2-layer FR4 PCB
Interface	12 SMA connectors and
Input power	3.3V to 5V DC