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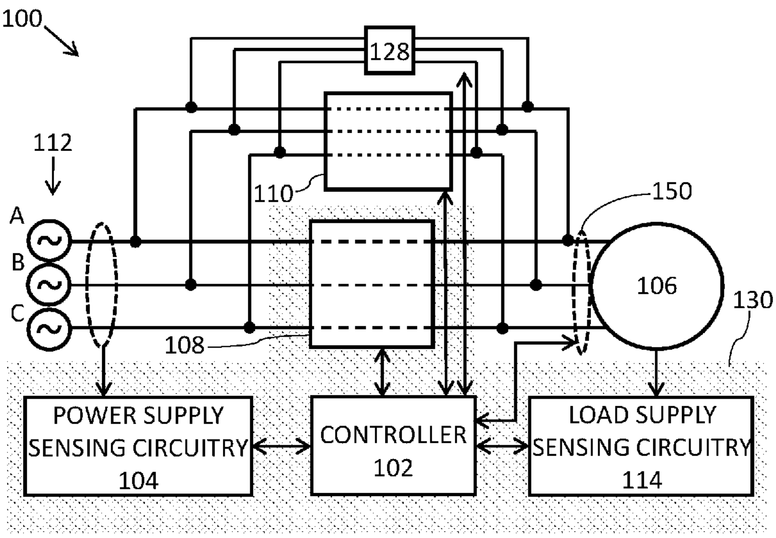


FIG. 1

(57) Abstract: A method of transitioning between supplying electrical power from a three phased supply to a load through three activated electrical supply pathways of a first supply module, to supplying power to the load through three activated electrical supply paths of a second supply module, including: monitoring a sector of the three phase supply; selecting a first phase for transition, based on the sector; and activating a first pathway through the second supply module, corresponding to the first phase and deactivating a first pathway through the first supply module corresponding to the first phase, while at least one pathway of the first supply module remains activated.

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# COMMUTATION BETWEEN GRID AND INVERTER

## TECHNOLOGICAL FIELD

The present disclosure, in some embodiments, thereof, relates to commutation strategies and, more particularly, but not exclusively, to commutation between inverter powering and grid powering of a load.

## BACKGROUND ART

US Patent No. US10,778,122B2 discloses *"A connecting device for motor and supply network is provided, comprising: a Variable Frequency Drive (VFD), a first switch (S1) and a second switch (S2), wherein the Variable Frequency Drive (VFD) is connected in series to the first switch (S1), and the second switch (S2) is connected in parallel to the series circuit composed of the Variable Frequency Drive (VFD) and the first switch (S1). The connecting device of the invention further comprises a bidirectional Silicon Controlled Rectifier (SCR) or two anti-parallel single-directional Silicon Controlled Rectifiers (SCR1,SCR2), wherein the bidirectional Silicon Controlled Rectifier (SCR) or the two anti-parallel single-directional Silicon Controlled Rectifiers (SCR1,SCR2) is/are connected in parallel to the second switch (S2). The connecting device of the present invention would not be subject to high current surge when VFD bypassing, avoids the high cost for the overrating of the cable and the bypassing switch, and is easy to be implemented."*

US Patent No. US10,594,246B2 discloses *"A motor control system for selectively controlling power from a power source to a load is provided. The motor control system includes at least one PCB structure and a plurality of protection and control components mounted onto the at least one PCB structure so as to be electrically coupled therewith. The plurality of protection and control components includes a power converter operable to provide a controlled output power to the load, a plurality of switching devices operable to selectively control power flow from the power source into the power converter and to bypass the power converter, and one or more protection devices configured to selectively* *interrupt current flow from the power source to the power converter during a fault condition. The motor control system also includes a housing enclosing the at least one PCB structure and the plurality of protection and control components."*

Additional background art includes US Patent No. US11,177,648B2, US Patent No. US11,139,649B2, CN101814873B, US Patent No. US10,247,162B2, and US Patent No. US9,018,882B2

Acknowledgement of the above references herein is not to be inferred as meaning that these are in any way relevant to the patentability of the presently disclosed subject matter.

## GENERAL DESCRIPTION

Following is a non-exclusive list of some exemplary embodiments of the disclosure. The present disclosure also includes embodiments which include fewer than all the features in an example and embodiments using features from multiple examples, even if not listed below.

Example 1. A method of transitioning between supplying electrical power from a three phased supply to a load through three activated electrical supply pathways of a first supply module, to supplying power to the load through three activated electrical supply paths of a second supply module, comprising:

monitoring a sector of said three phase supply;

selecting a first phase for transition, based on said sector; and

activating a first pathway through said second supply module, corresponding to said first phase and deactivating a first pathway through said first supply module corresponding to said first phase, while at least one pathway of said first supply module remains activated.

Example 2. The method according to Example 1, comprising selecting a second phase for transition, based on said sector;

activating a second pathway through said second supply module, corresponding to said second phase and deactivating a second pathway through said first supply module corresponding to said second phase.

Example 3. The method according to Example 2, comprising selecting a third phase for transition, based on said sector;

activating a third pathway through said second supply module, corresponding to said third phase and deactivating a third pathway through said first supply module corresponding to said third phase.

Example 4. The method according to any one of Examples 2-3, wherein said selecting, said activating, and said deactivating for said first phase and said second phase are performed during a same power supply sector.

Example 5. The method according to any one of Examples 4, wherein, after a time delay corresponding to a sector duration, said activating, and said deactivating for said third phase is performed.

Example 6. The method according to any one of Examples 2-3, wherein said selecting, said activating, and said deactivating for said first phase and said second phase are performed during a same power supply sector.

Example 7. The method according to Example 6, wherein said selecting, said activating, and said deactivating for said first phase is performed in a first power supply sector;

wherein said selecting, said activating, and said deactivating for said second phase and said third phase is performed in a first power supply sector.

Example 8. The method according to any one of Examples 1-7, wherein said deactivating occurs after said activating.

Example 9. The method according to any one of Examples 1-8, wherein said first power supply module is an inverter, and wherein said second power supply module is a bypass module configured to deliver said power supply to said load.

Example 10. The method according to Example 9, wherein said inverter is a switched mode variable frequency power supply receiving three phase power from a grid supply.

Example 11. The method according to Example 3, wherein said deactivating for each of said first, second, and third phases is prior to said activating for each of said first, second, and third phases;

wherein said activating for each of said first, second, and third phases is performed in a different sector of said three phase supply.

Example 12. The method according to Example 11, wherein said second power supply module is an inverter, and wherein said first power supply module is a bypass module configured to deliver said power supply to said load.

Example 13. The method according to Example 12, wherein said inverter is a switched mode variable frequency power supply receiving three phase power from a grid supply.

Example 14. The method according to any one of Examples 11-13, wherein said activating for one or more of said first, second, and third phases is upon verifying said deactivating.

Example 15. The method according to Example 14, wherein said verifying comprises verifying that a measurement of current through a deactivated pathway is below a threshold.

Example 16. The method according to Example 15, wherein said verifying comprises receiving a measurement of said current through said deactivated pathway.

Example 17. A power supply system comprising:

a variable speed drive (VSD) configured to receive a three phase power supply and to deliver a variable frequency three phased power supply to a load through a plurality of VSD electrical pathways;

a bypass module configured to receive and deliver said three phased power supply to said load through a plurality of bypass electrical pathways;

a controller configured to control transition between supplying said load through said VSD and through said bypass module by generating control signals for activation and deactivation of said plurality of VSD electrical pathways and said plurality of bypass electrical pathways, which controller configured to:

identify a phase state of said three phase power supply;

select a first phase for transition, based on said phase state; and

activate a first bypass pathway and deactivate a first VSD pathway, while at least one VSD pathway remains activated; **or**

activate a first VSD pathway and deactivate a first bypass pathway, while at least one bypass pathway remains activated.

Example 18. A controller for a power supply system comprising a variable speed drive (VSD) configured to receive a three phase power supply and to deliver a variable frequency three phased power supply to a load through a plurality of VSD electrical pathways and a bypass module configured to receive and deliver said three phased power supply to said load through a plurality of bypass electrical pathways, the controller configured to:

control transition between supplying said load through said VSD and through said bypass module by generating control signals for activation and deactivation of said plurality of VSD electrical pathways and said plurality of bypass electrical pathways, which controller configured to:

identify a phase state of said three phase power supply;

select a first phase for transition, based on said phase state; and

activate a first bypass pathway and deactivate a first VSD pathway, while at least one VSD pathway remains activated; **or**

activate a first VSD pathway and deactivate a first bypass pathway while at least one bypass pathway remains activated.

Example 19. A controller configured to generate switching signals for commutation between a variable frequency drive (VFD) and a bypass module each connecting a three phase alternating current (AC) power supply to a load, where each of said VFD and said bypass module have first, second, and third, pathways respectively corresponding to first, second, and third phases of said power supply, the controller configured to:

monitor a sector of said three phase AC power supply;

activate, based on said sector, during said sector one or two pathways through said bypass module, and disconnect, during said sector, a corresponding one or two pathways through said VFD;

activate, in a subsequent sector, a remaining one or two pathways through said bypass module and disconnect, during said subsequent sector, a corresponding remaining one or two pathways through said VFD.

Example 20. The controller according to Example 19, wherein the controller is configured to disconnect said corresponding one or two pathways through said VFD after the one or two pathways through said bypass module have been activated.

Example 21. The controller according to any one of Examples 19-20, wherein the controller is configured to disconnect said remaining one or two pathways through said VFD after the one or two remaining pathways through said bypass module have been activated.

Example 22. The controller according to any one of Examples 19-21, wherein said controller is configured to verify that a voltage vector of power supplied to said load through said VFD is sufficiently aligned with a voltage vector of said power supply.

Example 23. A controller configured to generate switching signals for commutation between a variable frequency drive (VFD) and a bypass module each connecting a three phase alternating current (AC) power supply to a load, where each of said VFD and said bypass module have first, second, and third, pathways respectively corresponding to first, second, and third phases of said power supply, the controller configured to:

monitor a sector of said three phase AC power supply;

deactivate, based on said sector, a first pathway through said bypass module, and activate, once said first pathway is deactivated, a corresponding first pathway through said VFD.

Example 24. The controller according to Example 23, wherein said controller is configured to deactivate a second pathway through said bypass module, and activate, once said second pathway is deactivated, during a subsequent sector, a corresponding second pathway through said VFD.

Example 25. The controller according to Example 24, wherein said controller is configured to deactivate a third pathway through said bypass module, and activate, once said third pathway is deactivated, during a sector following said subsequent sector, a corresponding third pathway through said VFD.

Example 26. A controller configured to generate switching signals for a variable frequency drive (VFD) and a bypass module connecting a three phase alternating current (AC) power supply to a motor, the controller configured to:

monitor phase timing of said AC power supply;

switch between power supply to said motor through said VFD and power supply to said motor through said bypass module while continuously supplying power to said motor by, based on said phase timing, enabling current paths corresponding to less than all phases of said AC power supply through both said bypass module and said VFD.

Example 27. A commutation method comprising:

controlling frequency of three phase power supplied through a variable frequency drive (VFD), to a load, to match the frequency and phase of load consumption to the frequency and phase of a three phase grid supply;

maintaining timing of control signals to said VFD;

monitoring a sector of said three phase supply;

selecting a first phase for transition, based on said sector;

activating, over at least two sectors of a frequency of the grid, pathways through a bypass module, and deactivating pathways through the VFD, while maintaining at least one active pathway;

deactivating, over at least two sectors of a frequency of the grid, pathways through a bypass module, and activating pathways through the VFD, while maintaining at least one active pathway, using said timing of said control signals to said VFD.

Unless otherwise defined, all technical and/or scientific terms used within this document have meaning as commonly understood by one of ordinary skill in the art/s to which the present disclosure pertains. Methods and/or materials similar or equivalent to those described herein can be used in the practice and/or testing of embodiments of the present disclosure, and exemplary methods and/or materials are described below. Regarding exemplary embodiments described below, the materials, methods, and examples are illustrative and are not intended to be necessarily limiting.

Some embodiments of the present disclosure are embodied as a system, method, or computer program product. For example, some embodiments of the present disclosure may take the form of an entirely hardware embodiment, an entirely software embodiment (including firmware, resident software, micro code, etc.) or an embodiment combining software and hardware aspects that may all generally be referred to herein as a “circuit,” “module” and/or “system.”

Implementation of the method and/or system of some embodiments of the present disclosure can involve performing and/or completing selected tasks manually, automatically, or a combination thereof. According to actual instrumentation and/or equipment of some embodiments of the method and/or system of the present disclosure, several selected tasks could be implemented by hardware, by software or by firmware and/or by a combination thereof, e.g., using an operating system.

For example, hardware for performing selected tasks according to some embodiments of the present disclosure could be implemented as a chip or a circuit. As software, selected tasks according to some embodiments of the present disclosure could be implemented as a plurality of software instructions being executed by a computational device e.g., using any suitable operating system.

In some embodiments, one or more tasks according to some exemplary embodiments of method and/or system as described herein are performed by a data processor, such as a computing platform for executing a plurality of instructions.

Optionally, the data processor includes a volatile memory for storing instructions and/or data and/or a non-volatile storage e.g., for storing instructions and/or data. Optionally, a network connection is provided as well. User interface/s e.g., display/s and/or user input device/s are optionally provided.

Some embodiments of the present disclosure may be described below with reference to flowchart illustrations and/or block diagrams. For example illustrating exemplary methods and/or apparatus (systems) and/or and computer program products according to embodiments of the present disclosure. It will be understood that each step of the flowchart illustrations and/or block of the block diagrams, and/or combinations of steps in the flowchart illustrations and/or blocks in the block diagrams, can be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general-purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer or other programmable data processing apparatus, create means for implementing the functions/acts specified in the flowchart steps and/or block diagram block or blocks.

These computer program instructions may also be stored in a computer readable medium that can direct a computer (e.g., in a memory, local and/or hosted at the cloud), other programmable data processing apparatus, or other devices to function in a particular manner, such that the instructions stored in the computer readable medium can be used to produce an article of manufacture including instructions which implement the function/act specified in the flowchart and/or block diagram block or blocks.

The computer program instructions may also be run by one or more computational device to cause a series of operational steps to be performed e.g., on the computational device, other programmable apparatus and/or other devices to produce a computer implemented process such that the instructions which execute provide processes for implementing the functions/acts specified in the flowchart and/or block diagram block or blocks.

Some of the methods described herein are generally designed only for use by a computer, and may not be feasible and/or practical for performing purely manually, by a human expert. A human expert who wanted to manually perform similar tasks, might be expected to use different methods, e.g., making use of expert knowledge and/or the pattern recognition capabilities of the human brain, potentially more efficient than manually going through the steps of the methods described herein.

## BRIEF DESCRIPTION OF THE DRAWINGS

In order to better understand the subject matter that is disclosed herein and to exemplify how it may be carried out in practice, embodiments will now be described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

FIG. 1 is a simplified schematic of a power supply system, according to some embodiments of the disclosure;

FIG. 2 is a method of transitioning from powering a load through a first module to powering the load through a second module, according to some embodiments of the disclosure;

FIGs. 3A-E are a series simplified schematics illustrating transitioning of power supply to a load from through a variable frequency drive (VFD) to through a bypass module, according to some embodiments of the disclosure;

FIG. 4 is a method of transitioning power supply to a load from through a VFD to through a bypass module, according to some embodiments of the disclosure;

FIGs. 5A-E are a series simplified schematics illustrating transition from power supply to a load through a bypass module to through a variable frequency drive (VFD) according to some embodiments of the disclosure;

FIG. 6 is a method of transitioning power supply to a load from through a bypass module to through a VFD, according to some embodiments of the disclosure;

FIGs. 7A-B are flow charts of a detailed power supply method, according to some embodiments of the disclosure;

FIGs. 8A-B are simplified schematics of a power supply system, according to some embodiments of the disclosure;

FIG. 9 is a plot of supply voltage with angle, for a three phase power supply, according to some embodiments of the disclosure;

FIG. 10 is a diagram illustrating inverter input and output states, according to some embodiments of the disclosure;

FIGs. 11A-D are simplified schematics illustrating voltages for exemplary system states, according to some embodiments of the disclosure;

FIG. 12 is a plot of supply current and voltage to a load, with time, according to some embodiments of the disclosure;

FIGs. 13A-C are simplified schematics illustrating voltages for exemplary system states, according to some embodiments of the disclosure;

FIG. 14A is a plot of supply currents, with time, for dead time transition between inverter to grid;

FIG. 14B is a plot of motor currents, with time, for dead time transition between inverter to grid;

FIG. 14C is a plot of motor speed, with time, for dead time transition between inverter to grid;

FIG. 14D is a plot of motor torque, with time, for dead time transition between inverter to grid;

FIG. 15A is a plot of supply currents, with time, for transition between inverter to grid, according to some embodiments of the disclosure;

FIG. 15B is a plot of motor currents, with time, for transition between inverter to grid, according to some embodiments of the disclosure;

FIG. 15C is a plot of motor speed, with time, for transition between inverter to grid, according to some embodiments of the disclosure;

FIG. 15D is a plot of motor torque, with time, for transition between inverter to grid, according to some embodiments of the disclosure;

FIG. 16A is a plot of supply currents, with time, for dead time transition between grid to inverter;

FIG. 16B is a plot of motor currents, with time, for dead time transition between grid to inverter;

FIG. 16C is a plot of motor speed, with time, for dead time transition between grid to inverter;

FIG. 16D is a plot of motor torque, with time, for dead time transition between grid to inverter;

FIG. 17A is a plot of supply currents, with time, for transition between grid to inverter, according to some embodiments of the disclosure;

FIG. 17B is a plot of motor currents, with time, for transition between grid to inverter, according to some embodiments of the disclosure;

FIG. 17C is a plot of motor speed, with time, for transition between grid to inverter, according to some embodiments of the disclosure;

FIG. 17D is a plot of motor torque, with time, for transition between grid to inverter, according to some embodiments of the disclosure;

FIG. 18 is a simplified schematic of an exemplary implementation of a system, according to some embodiments of the disclosure; and

FIGs. 19A-C are plots of motor torque with time, for inverter to grid transitions, according to some embodiments of the disclosure.

In some embodiments, although non-limiting, in different figures, like numerals are used to refer to like elements, for example, element **106** in FIG. 1 corresponding to element **806** in FIG. 8A.

## DETAILED DESCRIPTION OF EMBODIMENTS

The present disclosure, in some embodiments, thereof, relates to commutation strategies and, more particularly, but not exclusively, to commutation between inverter powering and grid powering of a load.

### Overview

A broad aspect of some embodiments of the disclosure relates to commutation strategies having gradual transitions between supply of a three phase electrical power supply (e.g., grid supply e.g., supplied through a bypass module) to a three-phased load (e.g., motor including three coils, each coil corresponding to a phase) and a variable frequency three phase electrical power supply, also herein termed “variable frequency drive” and “inverter”. Where, during the transition, electrical supply to the load is maintained.

In some embodiments, one or more portion of the transition may be a “closed transition” where both the bypass module and the inverter are supplying the load in parallel. In some embodiments, parallel supply may be for a same phase of the three phase supply. In some embodiments, parallel supply may be where the inverter and bypass module are both supplying different phases to the load, at the same time. This may contrast with “open transition”, also termed “dead-time” transition techniques, where both the inverter and grid supplies (e.g., for all phases thereof) may be disconnected when transitioning therebetween.

In some embodiments, a controller controls delivery of power to the load, by controlling activation and deactivation of electrical pathways through the inverter and through the bypass module. Where, in some embodiments, control is via switches (e.g., including transistors) which receive control signals from the controller. In some embodiments, the control signals include voltages applied to gates of the transistors. Where, for example, an activating gate signal may allow and/or establish a current channel through the transistor switch and a deactivating gate signal may deplete and/or block a current channel through the transistor switch. Where switches are turned on or closed to activate a pathway, and turned off or opened to deactivate a pathway. For ease of description, reference will be hereinbelow to “activated”, and “deactivated” switches.

In some embodiments, timing of activation and deactivation of electrical pathways during the transition is based on polarities of the different phases of the electrical voltages and currents, where activation and deactivation of pathways and timing thereof is selected to supply power to the load continuously, but without producing short-circuit/s.

An aspect of some embodiments of the disclosure relates to transitioning between supplying a load via the inverter and supplying a load via the bypass module, where during the transition, power supply to the load is maintained e.g., through at least one electrical pathway of the inverter or bypass module.

In some embodiments, the inverter includes a switching unit receiving outputs of a rectifier connected to the three phase power supply, where the inverter has a switching leg corresponding to each phase of the three-phased load. In some embodiments, the controller controls the legs of the switching module to selectively deliver positive and negative voltages (and currents) to phases of the three-phase load to generate a load voltage vector.

In some embodiments, the transition occurs where at least one bypass module electrical pathway is activated while the inverter continues for example, for a short period of time (e.g., for 0.1-1000μs) to provide power to the load through all three legs of the inverter. In this situation, a phase of the bypass module and a corresponding phase of the inverter are activated at the same time, where, in some embodiments, a duration of this parallel supply may be of up to 120 degrees e.g., about 6.67ms (for 50Hz supply). In some embodiments, timing of activation of the bypass module electrical pathway/s and/or which phase pathways are activated is based on the power supply phase state e.g., to avoid short circuits. Where, a short circuit may occur when a leg of the inverter is delivering a polarity of voltage to a phase of the load and the bypass module is delivering a different polarity voltage supply to the phase of the load.

An aspect of some embodiments of the disclosure relates to transitioning from driving the load through the inverter to driving the load with the grid supply (e.g., through the bypass module) where, while the inverter (e.g., at least one leg thereof) is still supplying power to the load, one or two phases of the grid power supply are delivered to the load (e.g., through the bypass module).

In some embodiments, only after connecting the one or two phases of the grid power supply are the corresponding phase/s of the inverter disconnected. A potential advantage being reduction in time for which the load is not powered for all phases. Where, in some embodiments, a delay between connecting the grid power supply and deactivating inverter phase pathways is of short duration.

In some embodiments, disconnection of corresponding phase/s of the inverter is at the same time as (or preceding) activation of phase pathway/s of the grid power supply e.g., through the bypass module. A potential advantage being prevention of short-circuit/s through the inverter.

Then, in some embodiments, the third and final phase is connected e.g., following a same procedure where the third phase of the grid supply is connected and then the third phase of the inverter is disconnected. Timing of stages of the process and/or selection of phases in the process may be based on the identified stage within the three phase grid power supply. In some embodiments, inverter leg disconnection occurs during a same voltage input sector as that in which the corresponding bypass phase is activated. Where voltage input sectors are each a sixth of a full grid power supply cycle (e.g., where the power supply oscillates at 50Hz, a sector has 3.3ms duration) where each sector corresponds to two phases being, for the entire sector, different polarity.

In some embodiments transitioning from driving the load through the grid (e.g., via the bypass module) to driving the load with the inverter is performed according to a reverse procedure as that described regarding inverter to grid transition. For example, where two phases may be activated and deactivated at once. For example, in embodiments, where the bypass module includes MOSFET and/or IGBT transistors.

An aspect of some embodiments of the disclosure relates to transitioning from grid supply driving of a load (e.g., through a bypass module) to driving the load through an inverter, where, a phase of the inverter is connected, while the grid is still supplying power to the load via one or more electrical pathways through the bypass module (e.g., through pathway/s of the bypass module associated with phases other than the phase for which the inverter has been connected).

In some embodiments, (e.g., associated with a type of switch used in the bypass module e.g., when the bypass module includes thyristor switches) control signals are timed so that a bypass module electrical pathway corresponding to a phase is disconnected prior to connection of a corresponding pathway of the inverter.

For example, in some embodiments, timing of control signals for switches take into account a delay between opening/closing of a switch and the switch receiving a control signal instructing the opening/closing. For example, where the bypass module includes thyristors, which deactivate only after the thyristor has received a control signal (e.g., at the thyristor gate) instructing the thyristor switch to deactivate and current through the thyristor has dropped to zero (or below a threshold value).

In embodiments where bypass switching is sufficiently rapid (e.g., a bypass electrical pathway is disabled within a single sector of the grid power supply), transition between the bypass to the inverter, in some embodiments, mirrors that as described hereinabove regarding transition from inverter to grid. For example, where one or two phases of the inverter are activated, and then the corresponding phases of the bypass module are deactivated e.g., after the activation of the inverter phase/s. Followed by the remaining one or two inverter phases being activated and corresponding phase/s of the bypass module being deactivated.

Before explaining at least one embodiment of the invention in detail, it is to be understood that the invention is not necessarily limited in its application to the details of construction and the arrangement of the components and/or methods set forth in the following description and/or illustrated in the drawings and/or the Examples. The invention is capable of other embodiments or of being practiced or carried out in various ways.

**Exemplary system**

FIG. 1 is a simplified schematic of a power supply system **100**, according to some embodiments of the disclosure.

In some embodiments, power supply system **100** includes a multi-phase power supply e.g., a fixed frequency power supply (FFPS) **112**, also herein termed a “grid supply” or just “grid”. In some embodiments, power from grid supply **112** is supplied to a load **106** via a plurality of routes controlled by a controller **102**. In some embodiments, load **106** includes an electric motor, for example, a motor which rotates at a speed associated with that of the grid supply (e.g., synchronous motor (electrically excited synchronous motor, permanent magnet synchronous motor, synchronous reluctance motor) or induction motor). At a given rating, synchronous motors may lose less energy than induction motors.

It should be noted, that, although in practice, frequency of the grid supply may fluctuate, the grid supply frequency is not controlled by controller **102**.

In some embodiments, the plurality of routes include grid power passing to load **106** through variable frequency drive (VFD) **108**, also herein termed “inverter” which may be controlled by controller **102**. In some embodiments, the plurality of routes includes grid power passing to load **106** through a bypass module **110**. Optionally, in some embodiments, the plurality of routes includes grid power passing to load **106** through a relay module **128**.

In some embodiments, relay module **128** includes a plurality of relay switches. For example, including high-power relays and/or contactors for each phase of the power supply.

In some embodiments, bypass module **110** includes a plurality of switches e.g., a switch for each phase of power supply e.g., each switch including two anti-parallel connected transistors. In some embodiments, one or more transistor of the switches of bypass module **110** is a thyristor.

Optionally, in some embodiments, current flowing through pathways (and/or voltage across) of bypass module **128** and/or to load **106** are measured and/or monitored.

For example, where one or more current sensors **150** provide measurement/s to controller **102**. In some embodiments, sensor/s **150** are positioned just up-stream of load **106**, e.g., to measure motor input currents supplied either by inverter **108** or bypass **110** module. Where, in some embodiments, the measurement/s are used to verify that the pathway/s are deactivated e.g., to verify that current through the thyristors has fallen to zero.

In some embodiments, one or more voltage sensor/s measure voltage at load **106** and/or at one or more additional portion of system **100**. For example, where load supply sensing circuitry **114** is configured to measure voltage of electrical supply received by load **106**.

As will be detailed hereinbelow, controller **102** controls passage of power through the plurality of routes by controlling switching elements (e.g., including semiconductor switches, e.g., transistors) within bypass module **110** and/or VFD **108** and/or relay module **128**.

In some embodiments, controller **102** controls inverter **108** (e.g., controlling switching of transistors of the inverter e.g., as described regarding FIGs. 8A-B) to control frequency and/or magnitude of voltage supplied to load **106**.

In some embodiments, control is based on (e.g., controller **102** generates control switching signals based on) measurement/s received from one or more sensor **104**, **114**, **150**. Where, in some embodiments, system **100** includes power supply sensing circuitry **104** configured to measure feature/s of grid supply **112**.

In some embodiments, one or more elements of system **100** are hosted in a same housing and/or device **130**. Where, for example, in some embodiments, one or more of inverter **108**, controller **102**, power supply sensing circuitry **104**, and load supply sensing circuitry **114** are provided in a single housing and/or as a single microcontroller.

In some embodiments, bypass module **110** and relay module **128** are hosted in a same housing and/or device. Optionally, in some embodiments, the bypass module is hosted in a device or element which also includes sensing circuitry configured to provide measurements e.g., of voltage and/or current to the controller.

**Exemplary methods**

FIG. 2 is a method of transitioning from powering a load through a first module to powering the load through a second module, according to some embodiments of the disclosure.

At **200**, in some embodiments, a load (the load, for example, including one or more feature of load **106** FIG. 1) is powered by a first module where the load receives a three phase power through three activated electrical pathways of the first module.

At **202**, in some embodiments, a first electrical pathway through a second module is activated, while at least one electrical pathway through the first module remains activated.

At **204**, in some embodiments, the first module first electrical pathway is deactivated.

In some embodiments, the deactivation is prior to activation of the first electrical pathway through the second module e.g., as illustrated by dashed arrows in FIG. 2, e.g., where the first module is a bypass having thyristor switches.

In some embodiments, the deactivation is at a same time as or after the activation e.g., as illustrated by solid line arrows in FIG. 2.

At **206**, in some embodiments, steps **202**-**204** are repeated for second and third pathways corresponding to second and third phases of the electrical supply.

At **208**, the load is powered through the second module, receiving three phases through three activated electrical pathways of the second module.

In this method a first and a second module are described, where each module provides power to a load, where the method is of transitioning from power supply through one module to another.

Where, in some embodiments, the first module is an inverter (e.g., including one or more features of inverter **108** FIG. 1 and/or inverter **808** FIGs. 8A-B) and the second module is a bypass module (e.g., including one or more features of bypass module **110** FIG. 1 and/or bypass module **810** FIGs. 8A-B). Where, in some embodiments, the first module is a bypass module and the second module is an inverter.

In some embodiments, for example, depending on a speed at which electrical pathways are deactivated (e.g., step **204** e.g., as described herein below in more detail), in some embodiments, step **202** may include activating two electrical pathways through the second module, and step **204** may include deactivating the corresponding two electrical pathways in the first module.

FIGs. 3A-E are a series simplified schematics illustrating transitioning of power supply to a load **306** from through a variable frequency drive (VFD) **308** to through a bypass module **310**, according to some embodiments of the disclosure.

FIG. 4 is a method of transitioning power supply to a load from through a VFD to through a bypass module, according to some embodiments of the disclosure.

At **400**, and, for example, illustrated by FIG. 3A, power is supplied to a load through an inverter where, for example, a bypass module is disabled.

At **402**, and, for example, illustrated by FIG. 3B, based on a time point in the three phases of a grid supply **312**, two phases of grid supply are connected (as indicated by solid lines) through bypass module **310** where inverter **308** remains connected, for all three phases. Where connection of phases is also herein termed “activation of electrical pathways”.

In some embodiments, the time point in the three phases and/or the two phases are selected (e.g., by a controller e.g., controller **102** FIG. 1, controller **802** FIG. 8B) based on signal/s received by the controller for example, from power supply sensing circuitry (e.g., power supply sensing circuitry **104** FIG. 1).

At **404**, and, for example, illustrated by FIG. 3C, in some embodiments, the corresponding inverter pathways to those activated for bypass module **310** at step **402** are deactivated. In some embodiments, step **404** occurs prior to or concurrent with step **402**.

At **406**, and, for example, illustrated by FIG. 3D, in some embodiments, based a time point in the three phases of grid supply **312**, a third and final pathway through bypass module **310** is activated, e.g., optionally, where the third pathway through inverter **308** remains active.

At **408**, and, for example, illustrated by FIG. 3E, in some embodiments, the third and final path through inverter **308** is deactivated. In some embodiments, step **408** occurs prior to or concurrent with step **406**.

At **410**, (e.g., illustrated in FIG. 3E) the transition is now complete, power is supplied to load **306** only through bypass module **310** and not through inverter **308**.

In some embodiments, alternatively to activating and deactivating pathways for two phases of the power supply, then activating and deactivating pathways for the remaining phase, in some embodiments, a pathways for a single phase are activated (step **402**) and deactivated (step **404**). Where, subsequently, pathways for the two remaining phases are then activated (step **406**) and deactivated (step **408**).

The method of FIG. 4 illustrates exemplary embodiments, where pathways for two phases are activated through bypass module **310** at once. However, embodiments where a pathway for a single phase is activated at a time, for example, there being a delay between activation of each pathway (and deactivation of a corresponding inverter pathway) through bypass **310** are envisioned and encompassed.

FIGs. 5A-E are a series simplified schematics illustrating transition from power supply **512** to a load **506** through a bypass module **510** to through a variable frequency drive (VFD) **508** according to some embodiments of the disclosure.

FIG. 6 is a method of transitioning power supply to a load from through a bypass module to through a VFD, according to some embodiments of the disclosure.

At **600**, and, for example, illustrated by FIG. 5A, power is supplied to a load through a bypass module where, for example, a VFD is disabled (e.g., each electrical power supply pathway through VFD is disabled).

At **602**, and, for example, illustrated by FIG. 5B, based on a time point in the three phases of grid supply **512**, a single phase of bypass module **510** is deactivated. Where other phases of bypass module **510** remain activated.

At **604**, and, for example, illustrated by FIG. 5C, based on a time point in the three phases of grid supply **512**, a corresponding phase of VFD **508** to that deactivated in bypass module **510** at step **602** is activated.

At **606**, and, for example, based on a time point in the three phases of the grid supply, steps **602** and **604** are repeated for the other two phases. Where, in some embodiments, FIG. 5D illustrates the system after step **606** has been performed.

At **608**, and, for example, illustrated by FIG. 5E, power supply to load **506** is through VFD **506**, where all of pathways through bypass module **510** are deactivated.

FIGs. 5A-E and FIG. 6 correspond to embodiments where (e.g., associated with deactivation characteristics of thyristor switch/es of a bypass module) deactivation of bypass phase pathways and corresponding activation of inverter phase pathways is one at a time. However, in some embodiments, (e.g., where the bypass module includes transistors which deactivate more rapidly than thyristors e.g., includes IGBTs and/or BJTs and/or MOSFETs) deactivation of bypass phase pathways and corresponding activation of inverter phase pathways may be performed for two phases at once e.g., corresponding to a reverse of the procedure described regarding FIGs. 3A-E and/or FIG. 4.

FIGs. 7A-B are flow charts of a detailed power supply method, according to some embodiments of the disclosure.

Referring to FIG. 7A, at **700**, in some embodiments, initially, a load e.g., a motor is stationary and/or is not receiving electrical power. Although other types of load are envisioned and encompassed by this disclosure, discussion herein below will be with respect to a motor, and power supply to motor coils.

At **701**, according to some embodiments, switching of transistors of an inverter (e.g., of switching module **820** FIGs. 8A-B) is controlled to supply a variable magnitude and variable frequency voltage to the motor. For example, to accelerate the motor (e.g., rotation of the motor rotor) with controlled current.

In some embodiments, switching of the transistors controllably delivers positive or negative voltage to coils of the motor, where the polarity and duration of pulses delivered to coils is controlled to provide a selected frequency power supply to the coils. In some embodiments, the supply received at the motor coils provides a rotating magnetic field (e.g., to drive rotational of the motor). Where, in some embodiments, the frequency of the rotating magnetic field is related to speed at which rotor/s of the motor rotate.

In some embodiments, control of pulses delivered is according to a Pulse Width Modulation (PWM) scheme e.g., Space Vector Modulation (SVM), Sinusoidal Pulse Width Modulation (SPWM) with optional 3rd harmonic injection/compensation.

In some embodiments, third harmonic injection is provided by measuring the voltage level at the effective ground (the effective ground also herein termed “DC link voltage mid-point”) at the inverter input at node **854** (or deriving the effective ground voltage level from measured supply voltages). Where control signals generated by the inverter controller (e.g., duty cycles of the PWM) are adjusted (e.g., the adjustment being “feed-forward compensation”) to compensate for fluctuation (e.g., at triple the grid frequency, hence “third harmonic”) in the effective ground level at the DC link (at node **854**) .

Alternatively, in some embodiments, third harmonic compensation, in some embodiments, is provided by hardware. Where, for example, a neutral cable connection (e.g., a connection between node **854** and node **856** FIG. 8A), where supply to the inverter as provided to by the DC link is grounded via the neutral cable e.g., potentially boosting the DC link voltage.

In some embodiments, switching of the transistors is controlled to provide power supply to the motor having increasing frequency e.g., to accelerate the motor to a speed compatible with the grid power supply frequency. In some embodiments, frequency for driving the motor (e.g., ramping up of speed of the motor) is using V/f control e.g., open loop V/f control. Where control of the frequency is employed to maintain a constant ratio between the motor voltage (which is for example, measured the measurements supplied to a controller e.g., measured by load supply sensing circuitry **114** FIG. 1) and frequency e.g., to provide constant (or low variation in) motor flux. A potential benefit of low variation in motor flux is reduced motor inrush current during start-up, which may affect the power supply and e.g., other device/s connected to the same power supply.

In some embodiments, for example, alternatively or additionally to employing V/f based control, closed loop vector control (e.g., closed loop sensor-less vector control) is employed. Where, closed loop vector control, in some embodiments, includes using machine back-EMF (e.g., using voltage measurements) to estimate rotor flux angle and e.g., therefrom estimating motor rotor position. The motor current may be controlled so that rotor flux and motor current phasors intersect at a selected angle (e.g., 90 degrees). A potential benefit of which is that motor torque may be maximized with minimal inrush current to the motor.

In an exemplary embodiment, both V/f control and closed loop vector control are employed. Where, for an initial part of the acceleration of the motor, V/f control is employed, and then for the higher frequency portion of the acceleration sensor-less vector control is employed. Where, for example, acceleration from 0Hz-5Hz is implemented using V/f control and from 5Hz-grid frequency up to e.g., 50Hz, is sensor-less vector control. Where, a maximal acceleration may be achieved within 2 seconds at full power, e.g., if such accelerations are desired.

In an exemplary embodiment, closed loop vector control of the inverter provides an initial frequency of 2-10Hz, or about 5Hz, or lower or higher or intermediate ranges, or frequencies, and is ramped up to grid frequency (e.g., about 50Hz or about 60Hz) in 1--20s, or 1-15s, or about 10s, or within lower, or higher, or intermediate times, or ranges.

In some embodiments, once the frequency of the load voltages and currents supplied by the inverter is the same as (or sufficiently close to e.g., within 10mHz of) the grid frequency is reached, the phase of the inverter output is aligned to that of the grid. For example, by increasing and/or decreasing the inverter frequency. Where, in some embodiments, deviation of the inverter output frequency is maintained to within a threshold deviation of the grid frequency. Where, in an exemplary embodiment, a maximal allowed deviation is about 200mHz. In some embodiments, once the phase is synchronized, the inverter frequency is returned to the grid frequency. In some embodiments, phase matching is an iterative process where the inverter frequency is adjusted a plurality of times. In some embodiments, one or more phase locked loop (PLL) is used to track the phase of the inverter output voltage vector and/or grid voltage vectors where the phase error between the two voltage vectors is driven towards 0 e.g., using an integral controller.

At **702**, in some embodiments, feature/s of motor and/or inverter operation are verified. For example, verification is that the inverter generated output voltage vector matches the power supply input voltage vector. In some embodiment, e.g., prior to or as part of verifying, a time delay is introduced e.g., to allow transients (e.g., torque transients) to decay. A potential benefit being smoother transition.

At **703**, optionally, once synchronized, the inverter output is locked to the grid vector e.g., and will not lose synchronism, e.g., unless the inverter speed is reduced. In some embodiments, synchronism of the inverter output with the grid vector is maintained during supply via the grid, for example, potentially enabling transition from the grid to the inverter e.g., without re-synchronization step/s.

In some embodiments, an inverter locking procedure includes deriving a suitable inverter output voltage vector e.g., from the phase of the grid voltage vector directly. Where, in some embodiments, deriving of the inverter output voltage vector takes into account phase delays associated with measurement of the grid voltage vector and/or delay/s (e.g., digital delay) associated with generation by the inverter of switching control signals to provide suitable output voltage vectors. Where the measurement phase delay/s may include that introduced by analog to digital conversion (ADC) in supply of measurements of grid voltages to the inverter controller e.g., where ADC filter/s may introduce a phase delay.

At **704**, in some embodiments (e.g., upon verification in step **702**) based on a time point in the three phases of the power supply e.g., sector of the supply voltage, one or two paths through a bypass module are activated, for example, without deactivating the remaining path or paths (non-corresponding) of the inverter. For example, where phases A and B of the bypass module are activated, phase C of the inverter remains activated.

Optionally, in some embodiments, the activation of the bypass module path/s is carried out without deactivating corresponding paths through the inverter. For example, according to one or more feature of step **402** FIG. 4.

At **706**, in some embodiments, the corresponding inverter pathway/s to those activated at step **704** are deactivated e.g., according to one or more feature of step **404**

FIG. 4. In some embodiments, step **704** is performed prior to step **706**, a potential advantage being preventing inductive discharge peak/s in current associated with inductive currents e.g., of the motor windings.

Alternative, in some embodiments, steps **704** and **706** are performed at about the same time, or step **706** is performed prior to step **704**.

At **708**, in some embodiments, based on a time point in the three phases of the power supply, the remaining one or two path/s through the bypass module are activated, without deactivating corresponding path/s through the inverter. For example, according to one or more feature of step **406** FIG. 4.

At **710**, in some embodiments, the corresponding inverter pathway/s to those activated at step **708** are deactivated e.g., according to one or more feature of step **408** FIG. 4.

Potential benefit/s of disconnecting and/or deactivating switching of the inverter is reduction of introduced power losses and/or reduction of electromagnetic interference (EMI) signals associated with high voltage inverter transistor switching.

At **712**, optionally, in some embodiments, relay switches of a relay module (e.g., relay module **128** FIG. 1) are activated. After a time period (e.g., sufficient time to ensure the relays are latched, e.g., 5-**100** ms, or 5-50 ms, or lower, or higher, or intermediate ranges, or durations) pathways of the bypass module are deactivated.

In some embodiments, the bypass module switching is implemented using thyristors, a potential benefit of which is that activation of the bypass module may be more rapid than that of a relay module e.g., enabling a rapid switch over from inverter supply to grid supply via the bypass module. Where, for example, activation of bypass module thyristors (also herein termed “switching on”) is performed, for example, in about 1-5 µs, whereas reaction time of relays may be up to 5-50 ms. In some embodiments, relay switches of the relay module are activated/closed when bypass channels (e.g., thyristors) are fully activated/on. A potential benefit being, for example, what can be termed as the relays closing under a “soft switching” condition potentially reducing wear (e.g., associated with arching) on (potentially increasing lifetime of) the relays.

Now referring to FIG. 7B, at **714**, according to some embodiments, the motor is used e.g., in one or more of a fan, conveyer, belt, compressor, pump.

At **716**, according to some embodiments, for example, depending on feature/s of the use of the motor and/or motor features, the method splits into two paths, depending on whether a soft stop or reduction in speed for the motor is desired and/or required.

At **718**, in some embodiments, if a soft stop or reduction in speed of the motor is not required, relay switches (or bypass module switches in embodiments lacking a relay module) are deactivated. Power supply to the motor is then ceased and rotation of the motor ceases e.g., the motor coasting to a stop.

At **720**, optionally, for example, if the system includes a relay module, in some embodiments, pathways of the bypass module are activated and those of the relay module are deactivated.

At **721**, in some embodiments, the motor is powered via the bypass module. Where, for example, three bypass module pathways, one for each phase of the power supply, are activated.

At **722**, in some embodiments, a single pathway of the bypass module is deactivated e.g., by a controller (e.g., controller **102** FIG. 1) providing a deactivation control signal to the bypass module (e.g., to switch/s of the bypass module, e.g., gate voltage/s for one or more transistor of the bypass module) . Where, in some embodiments, e.g., as described regarding FIGs. 13A-C, there may be a delay between a switch of the bypass module pathway receiving a control signal instructing the deactivation of the switch and the pathway actually being deactivated e.g., without current flow therethrough.

At **724**, in some embodiments, a corresponding pathway of the inverter is activated.

In some embodiments, for example, to ensure that the pathway of the bypass module is deactivated, the corresponding pathway of the inverter is enabled a time delay after the deactivation control signal is sent to and/or received by the bypass module. In some embodiments, the time delay (e.g., associated with time required for bypass module switch/es to deactivate) corresponds to a fraction of a phase cycle of the grid supply, e.g., a time delay of 5°-30°, or about 15°, or up to a duration of a sector, 60°, where a full phase cycle is 360° e.g., refer to FIG. 9. In some embodiments, the time delay is selected to ensure that the pathway of the bypass module is closed, while having a minimal “dead” time duration where the power phase concerned is not provided to the load.

Optionally, in some embodiments, deactivation of the pathway of the bypass module is verified. Where, in some embodiments, deactivation is verified if current flow through the pathway drops to zero, and/or to below a threshold, the threshold also herein termed “holding current”. Where, in an exemplary embodiment, holding current is **100**mA. For example, where, in embodiments including bypass module sensor/s (e.g., sensor/s **150** FIG. 1), verification (e.g., performed by a controller e.g. controller **102**, FIG. 1) is using measurements provided by the sensor/s.

Optionally, in some embodiments, for example, alternatively or additionally to enabling the inverter pathway after a time delay, step **724** is performed upon verification that the bypass module pathway has been deactivated.

At **726**, in some embodiments, steps **722**, **724** are repeated until each pathway of the bypass module is deactivated and each pathway of the inverter is activated.

In some embodiments, for example, alternatively to steps **722**, **724**, and **726**, for example, where the bypass module has MOSFET transistor switches, deactivation of the bypass module may include deactivation of two phases at one time, preceded or followed by deactivation of the third phase. Where the deactivation may be at the same time as activation of a corresponding leg of the inverter. The method, for example, mirroring, in reverse, that of transition between inverter to grid e.g., including (in reverse) feature/s of step/s **704**, **706**, **708**, **710**.

At **728**, in some embodiments, speed of motor rotation is controlled e.g., by control of switching at the inverter. For example, where in some embodiments, the motor speed is reduced gradually (e.g., more gradually than would occur if performing step **718**). For example, where in some embodiments, motor speed is reduced to a lower speed than that provided by the characteristic/s (e.g., frequency) of the grid power supply.

**Detailed exemplary system**

FIGs. 8A-B are simplified schematics of a power supply system **800**, according to some embodiments of the disclosure.

Includes one or more feature of system **100** FIG. 1, for example, a grid supply **812**, an inverter **808**, a load **806**, and a bypass module **810** each of which corresponding to grid supply **112**, inverter **108**, load **106**, and bypass module **110** of FIG. 1.

For ease of illustration, controller/s **802a**, **802b** are not illustrated in FIG. 8A, but are illustrated in FIG. 8B.

In some embodiments, grid supply **812** provides a three phase power supply as illustrated by three power sources **A**, **B**, **C**. Where, in some embodiments, the supply is grounded **856**.

In some embodiments, inverter **808** includes a rectifier module **816** having diodes **D1-D6**, and a switching module **820** having transistors **T1-T6**. Where, in some embodiments, rectifier module **816** provides an input stage of inverter **808** and/or switching module **820** provides an output stage of inverter **808**.

Optionally, in some embodiments, rectifier module **816** and switching module **820** are connected via a DC link module **818**. Where, in some embodiments, the DC link module **818** includes one or more capacitors. In some embodiments, the DC link module **818** includes a plurality (e.g., two) of series connected capacitors. In some embodiments, the DC link module **818** includes a ground node **854**.

Optionally, in some embodiments, (and not illustrated) ground node **854** is connected to ground e.g. to ground **856** by a neutral cable.

In some embodiments, one or more of inverter **808** transistors includes, (e.g., each of **T1-T6**) an insulated-gate bipolar transistor (IGBT).

In some embodiments, one or more of the inverter **808** transistors **T1-T6** includes one or more parallel connected component which allows current flow in a direction opposite to that enabled when the transistor is activated e.g., the one or more parallel connected component including a diode. For example, where transistor **T1** has a parallel connected diode **852**. In some embodiments the parallel connected components (e.g., diodes) provide discharge routes for stored electrical energy. For example, allowing discharge of one or more capacitive and/or inductive element. For example of inductive energy stored on motor coil/s **MA**, **MB**, **MC**.

In some embodiments, bypass module **810** includes a switch **ThA**, **ThB**, **ThC** per phase channel for each phase channel of grid power supply **812**. In some embodiments, the switches each include two anti-parallel connected switches, e.g., semiconductor switches, e.g., transistors. Where, in an exemplary embodiment, the two switches include two thyristors connected in anti-parallel. Anti-parallel connection enables supply through the switch in both directions e.g., to apply both positive and negative half-cycles of supply voltages to load **806**.

In some embodiments, load **806** is a three phase load having a load **MA**, **MB**, **MC** per phase of grid supply **812**. For example, where, in some embodiments, load **806** includes a motor (e.g., synchronous motor e.g., induction motor) where each of **MA**, **MB**, and **MC** include motor coils (e.g., stator coils).

Illustrated in FIG. 8B is controller circuitry **802a**, **802b** which may be hosted by more than one controller (e.g., as illustrated in FIG. 8B) or may be hosted by a single controller module. Where controller circuitry **802a**, **802b** controls switching signals (e.g. gate signals) for switching of bypass switches and/or switching of inverter switches. For example, where connections **822**, **824**, **826** respectively, carry gate control signals from controller **802b** for switching of transistors **T1**, **T2**, of phase A, transistors **T3**, **T4**, of phase B, and transistors **T5**, **T6**, of phase C.

Controller circuitry **802b**, in some embodiments, controls switching of transistors of switching module **820** of inverter **808** using one or more pulse width modulation (PWM) scheme. Where, in some embodiments, switching of transistors **T1-T6** is controlled to deliver positive and negative voltages to load portions **MA**, **MB**, **MC**. Where the switching is controlled to provide an effective selected frequency voltage e.g., using PWM.

To understand operation of the inverter circuit let us examine a single phase of grid supply **812**, phase A. When voltage from **A** is positive, **D1** is active allowing current from phase A to flow towards switching module **820**. Controlling switching of **T1** and **T2** controls when the phase A load coil **MA** receives this positive voltage. When voltage from grid supply **812** phase A is negative, switching of **T1** and **T2** controls when the phase A load coil **MA** receives this negative voltage.

FIG. 9 is a plot of supply voltage with angle, for a three phase power supply, according to some embodiments of the disclosure.

On FIG. 9 are annotated which diodes are conducting e.g., of diodes **D1-D6** corresponding, in some embodiments, to diodes **D1-D6** of FIGs. 8A-B, based on the polarity of the associated phase/s of the power supply. Sectors are also annotated, where each sector corresponds to 60 degrees or a sixth of a power supply cycle. Where each sector has a different combination of active diodes.

In FIG. 9, a peak of phase voltage A is designated 0°.

Referring back to FIGs. 8A-B, diode **D1** conducts between 300° and 60° as during this period phase voltage A is of the highest positive amplitude out of all three phases of the power supply. The conduction periods of diodes **D3** and **D5** correspond to when the phase voltages B and C are of the highest positive amplitude, respectively. The same principle applies for diodes D4, D6 and D2 conducting during the negative phase voltage amplitudes for phases A, B and C respectively. All diode conduction periods are of **120°** and overlap with two conduction periods of diodes from the opposite leg of the diode rectifier. For example, when **D3** from the upper leg of the rectifier conducts, it overlaps with the conduction periods of **D2** and **D4** from the lower leg of the rectifier. Hence, the inverter input can be split into six states or sectors, I-VI, marked on FIG. 9, a sector for each 60°. During each sector, two diodes are conducting and connecting two supply voltage phases e.g., referring to FIGs. 8A-B, to an input of switching module **820** of inverter **808**.

FIG. 10 is a diagram illustrating inverter input and output states, according to some embodiments of the disclosure.

Referring back to FIG. 8A, in some embodiments, rectifier module **816** e.g., along with DC link **818** provides positive DC link voltage or the negative DC link voltage to the inverter input, where switching of transistors of switching module **820** controllably delivers the positive and negative DC link voltage to motor coils MA, MB, MC. Referring to FIG. 9, the positive and negative voltages supplied by the rectifier module (e.g., to the DC link) respectively, may be upper and lower envelopes of the three phases together illustrated in FIG. 9. In some embodiments, an effective ground produced (e.g., at node **854** FIG. 8) may fluctuate e.g., with the envelopes (e.g., at triple the grid frequency).

In some embodiments, switching is controlled to provide power to the motor coils which generates a rotating magnetic field (e.g., to drive rotation of the motor). By controlling switching of the inverter transistors the frequency of the rotating magnetic field, and that of the motor may be controlled.

FIG. 10 illustrates output states V000-V111 of the inverter corresponding to the rotating magnetic field of the motor, along with input states to the inverter, of the power supply, sectors I-VI.

Where the hexagon illustrated in FIG. 10 represents an output voltage range of the inverter with the corresponding discrete output states (also herein termed “space vectors” illustrated with arrows) of the inverter.

For example, arrow V100 represents an inverter output state, where, referring to FIG. 8A phase A has the high-side of the inverter leg **T1** activated, applying positive DC link voltage to motor winding A MA. Phases B and C have the low-side of the inverter legs **T4**, **T6** activated, delivering negative DC link voltage to motor windings B and C respectively **MB**, **MC**.

Space in between the discrete space vectors (illustrated as arrows) represents a combination of the two adjacent inverter output states. For example, in sector VI the inverter output state varies between 'V001' and 'V101'. The null vectors 'V000' and 'V111' may also be applied in each sector e.g., depending on the desired voltage amplitude.

In FIG. 10, the two circles represent the conduction periods of the diodes in the rectifier. The inner circle represents the upper diodes (**D1**, **D3** and **D5**, FIG. 8A), while the outer circle represents the lower diodes (**D2**, **D4**, and **D6**, FIG. 9B).

The diagram shown is in the synchronized state, where the inverter is synchronized to the grid frequency.

The inverter output states consist of eight configurations of the inverter's six transistors **T1-T6**. These eight output states are denoted by V000-V111. For each inverter phase leg, only one transistor may be active/switched on at any time. Hence, the configuration V110 represents the configuration where transistors **T1**, **T3** and **T6** are activated and **T2**, **T4** and **T5** are deactivated. The configurations or voltage vectors V000 and V111 represent the null vectors, as during these voltage vectors the motor windings are short-circuited.

Table 1 also shows relationships between inverter input state (sector), inverter output state (voltage vectors), which diodes are active.

*Table 1*

| Sector | Voltage vectors | Diodes |
|---|---|---|
| I | V101 V100 | D1 D6 |
| II | V100 V110 | D1 D2 |
| III | V110 V010 | D3 D2 |
| IV | V010 V011 | D3 D4 |
| V | V011 V001 | D5 D4 |
| VI | V001 V101 | D5 D6 |

**Exemplary transition from inverter to grid**

FIGs. 11A-D are simplified schematics illustrating voltages for exemplary system states, according to some embodiments of the disclosure.

In some embodiments, FIGs. 11A-D illustrate a power supply system **1100** which includes one or more feature of system **100** FIG. 1 and/or system **800** FIGs. 8A-B. For example, where a bypass module **1110** including switches ThA, ThB, ThC includes one or more feature of bypass module **110** FIG. 1 and/or bypass module **810** FIGs. 8A-B. For example, where a power supply **1112** includes one or more feature of power supply **112** FIG. 1 and/or power supply **812** FIGs. 8A-B. For example, where an inverter **1108** including a rectifier **1116** and a switching module **1120** includes one or more feature of inverter **108** FIG. 1 and/or rectifier **1116** and/or switching module **1120** including one or more feature of rectifier **816** and/or switching module **820** FIGs. 8A-B respectively. For example, where a load **1106** includes one or more feature of load **106** FIG. 1 and/or load **806** FIGs. 8A-B.

For simplicity of illustration, in FIGs. 11A-D switches **T1-T6** of an inverter **1108** and switches **ThA**, **ThB**, **ThC** of bypass module **1110** are illustrated as either closed or open current paths. Where the opening/closing of the switches is controlled by a controller (e.g., controller FIG. 1). For simplicity of illustration, diodes **D1-D6** of rectifier **1116** are illustrated as either closed or open (corresponding to conducting and non-conducting/reverse biased states, associated with polarity of the connected power supply/ies and the diode electrical orientation).

Referring now to FIG. 11A which, in some embodiments, illustrates where, e.g., according to step **402** FIG. 4 where two phases are both connected through the bypass module **1110** and inverter **1108**.

In detail; both phase A and phase B pathways through bypass module **1110** are activated, where phase A of the power supply passes through switch ThA and phase B passes through switch **ThB**. While switching module **1120** is in a <u>V100 inverter state</u>, with transistors **T1**, **T4**, <u>**T6**</u> activated and transistors **T2**, **T3**, and <u>**T5**</u> are deactivated. The power supply is also within <u>sector I</u> where phase A of power supply **1112** is positive, phase B is negative, and phase C transitions from positive to negative. Corresponding to polarities of phases A and B, diodes **D1** and **D6** are conducting meaning that load **1106** is receiving power supply phases A and B both through bypass module **1110** and through inverter **1108**. Where phase A current paths/voltage supply is illustrated with heavy solid lines, and phase B current paths/voltage supply is illustrated with heavy dotted lines. Considering phase C, short circuiting does not occur for either polarity, positive polarity of phase C supply passing into the inverter path of phase A, and negative polarity of phase

C supply passing into the inverter path of phase B. In some embodiments, switching module legs associated with phase A and B are deactivated (**T1**, **T2**, **T3**, and **T4** are disabled) during the sector in which the phase A and B bypass pathways via **ThA**, **ThB** are activated.

Referring now to FIG. 11B which, in some embodiments, illustrates why, in some embodiments, activation of all three pathways through the bypass module **1110** and inverter **1108** is not performed e.g., potentially preventing short circuiting of phases of the power supply.

In detail, FIG. 11B illustrates a same situation as that illustrated in FIG. 11A where the inverter state is V100, and the power supply is in sector I. However, in FIG. 11B, bypass module **1110** pathway for phase C is activated with switch ThC closed. This results in a short circuit at **1132** where, for example, at the beginning of sector I positive polarity of phase C meets negative polarity of phase B.

Referring now to FIG. 11C which, in some embodiments, illustrates another inverter state, V101 where, e.g., according to step **402** FIG. 4 where two phases are both connected through the bypass module **1110** and inverter **1108**. V101, in some embodiments, is the second voltage vector present in Sector I, apart from V**100**.

In detail; both phase A and phase B pathways through bypass module **1110** are activated, where phase A of the power supply passes through switch **ThA** and phase B passes through switch **ThB**. While switching module **1120** is in a <u>V101 inverter state</u>, with transistors **T1**, **T4**, <u>**T5**</u> activated and transistors **T2**, **T3**, and <u>**T6**</u> are deactivated. The power supply is also within <u>sector I</u> where phase A of power supply **1112** is positive, phase B is negative, and phase C transitions from positive to negative. Corresponding to polarities of phases A and B, diodes D1 and D6 are conducting meaning that load **1106** is receiving power supply phases A and B both through bypass module **1110** and through inverter **1108**. Where phase A current paths/voltages are illustrated with heavy solid lines, and phase B current paths/voltages are illustrated with heavy dotted lines. Considering phase C, short circuiting does not occur for either polarity, positive polarity of phase C supply passing into the inverter path of phase A, and negative polarity of phase C supply passing into the inverter path of phase B.

Referring now to FIG. 11D which illustrates later activation of the final bypass module pathway. Where FIG. 11D illustrates sector II of the power supply (subsequent to sector I) and both inverter states V100 and V110.

Corresponding, for example, to completion of step **404** of FIG. 4, inverter pathways for both phase A and B have been deactivated and all of transistors **T1**, **T3**, **T2**, and **T4** are deactivated.

**Exemplary transition from grid to inverter**

FIG. 12 is a plot of supply voltage and current to a load, with time, according to some embodiments of the disclosure.

FIG. 12, in some embodiments, illustrates supply voltage and current to an exemplary load having an exemplary inductance when the load is grid-supplied (e.g., not power-supplied by the inverter). Where in FIG. 12, time for both plots is aligned. On FIG. 12, sectors I-VI e.g., as described regarding diode conduction and/or regarding FIG. 9 and/or FIG. 10 are illustrated. FIG. 12 illustrates lag of the current with respect to the voltage, the lag, for example, associated with motor inductance. Where, the lag is visible, for example, as a slight misalignment of sinusoids of the current with respect to the voltage.

FIGs. 13A-C are simplified schematics illustrating voltages for exemplary system states, according to some embodiments of the disclosure.

In some embodiments, FIGs. 13A-D illustrate a power supply system **1300** which includes one or more feature of system **100** FIG. 1 and/or system **800** FIGs. 8A-B and/or system **1100** FIGs. 11A-D. For example, where a bypass module **1310** including switches ThA, ThB, ThC includes one or more feature of bypass module **110** FIG. 1 and/or bypass module **810** FIGs. 8A-B and/or bypass module **1110** FIGs. 11A-D. For example, where a power supply **1312** includes one or more feature of power supply **112** FIG. 1 and/or power supply **812** FIGs. 8A-B and/or power supply **1112** FIGs. 11A-D. For example, where an inverter **1308** including a rectifier **1316** and a switching module **1320** includes one or more feature of inverter **108** FIG. 1 and/or rectifier **1316** and/or switching module **1320** including one or more feature of rectifier **816** and/or switching module **820** FIGs. 8A-B respectively. For example, where a load **1306** includes one or more feature of load **106** FIG. 1 and/or load **806** FIGs. 8A-B and/or load **1106** FIGs. 11A-D.

For simplicity of illustration, in FIGs. 13A-D switches T1-6 of an inverter **1308** and switches ThA, ThB, ThC of bypass module **1310** are illustrated as either closed or open current paths. Where the opening/closing of the switches is controlled by a controller (e.g., controller FIG. 1). For simplicity of illustration, diodes **D1-D6** of rectifier **1316** are illustrated as either closed or open (corresponding to conducting and non-conducting/reverse biased states, associated with polarity of the connected power supply/ies and the diode electrical orientation).

In some embodiments, switching at bypass module **1310** is by thyristors, timing of control signals instructing deactivation of the thyristors for deactivation of bypass module pathways and activation of corresponding pathways of inverter **1308** are timed so that the thyristors are no longer conducting when the inverter pathway is activated. For example, to prevent short circuiting of phases of the power supply.

For example, as described in more detail hereinbelow, in some embodiments, a bypass pathway is deactivated prior to activation of a corresponding inverter pathway, where, in some embodiments, timing of control signal/s for deactivation of the bypass pathway is based on a phase lag of motor current with respect to motor voltage, which may be dependent on the motor inductance.

Referring now to FIG. 13A which illustrates system **1300** during an exemplary sector I of the input supply, where a phase A bypass pathway has been deactivated e.g., by sending a control signal to ThA in sector VI prior to zero crossing **1200** FIG. 12 of current of phase A. In some embodiments, control signals are initiated for switching of phase A portions of switching module **1320** (**T1** and **T2**). Where control signals, in some embodiments, include PWM signals. Control signals for switching module portions related to phases B and C are still disabled where both possible voltage vectors V100 and V101 result in only **T1** being switched on, e.g., as shown in FIG. 13A.

Bypass module switch for phase C may be disabled in this sector (sector I), e.g., in preparation for the following sector.

Referring now to FIG. 13B which illustrates a short circuit **1332** between phases A and B. This scenario may occur, for example, if the control signal to deactivate thyristor switch **ThA** is received after the zero crossing for the current of phase A. For example, if, in sector I both the phase A inverter path is activated (**T1** on) and **ThA** is instructed to deactivate, **ThA** will remain activated (e.g., conducting) until the next zero crossing of current of phase A, which referring back to FIG. 12, is at **1202** in sector III. FIG. 13B illustrates short circuit **1332** occurring, in sector III prior to this zero crossing **1202**. Where, since in sector III phase B is positive, **D3** being active, **T1** is activated, and phase A is negative.

If phase A of the inverter output is to be connected during sector I, then the thyristor gate signals for phase A are disabled during sector VI in order to allow their current to reach 0A.

This procedure is repeated for each phase with the next zero-crossing occurring for phase C, followed by phase B.

Referring now to FIG. 13C, which illustrates system **1300** during sector II for both V**100** and V**110** voltage vectors, as control signals for switching module phase B (**T3** and **T4**) remains disabled. Phase C of inverter output **1320** has been enabled, after deactivating of bypass module pathway for phase C (ThC) in the previous sector.

For example, in preparation for the last sector to complete the transition, the gate signal for the phase B thyristor is then disabled. In some embodiments, once the power supply enters sector III control signals for switching module **1320** phase C (**T5** and **T6**) is enabled e.g., to complete the transition from the grid to the inverter connected operation.

Although a transition where first phase A, then phase B, and then phase C are transitioned from bypass supply to inverter supply sequentially has been described, other orders e.g., B-C-A, or C-A-B are envisioned and encompassed. In an exemplary embodiment, transitions are in sequential sectors, a potential benefit being maintained motor current and/or torque with minimal disturbance during the transition.

**Exemplary current and motor features associated with exemplary transitions**

The figures referred to in this section (FIGs. 14A-17D) illustrate simulation results.

FIG. 14A is a plot of supply currents, with time, for open transition between inverter to grid.

FIG. 14B is a plot of motor currents, with time, for open transition between inverter to grid.

FIG. 14C is a plot of motor speed, with time, for open transition between inverter to grid.

FIG. 14D is a plot of motor torque, with time, for open transition between inverter to grid.

Referring to FIGs. 14A-B, the inverter outputs are disabled reflected in supply currents dropping to 0A at **1400** in FIG. 14A and motor currents dropping to 0A at **1402** in FIG. 14B. After a “dead time” **1406** of 5ms, the motor is connected directly to the supply through the bypass thyristors. This results in the motor currents no longer being modulated by the inverter switching. Both supply and motor currents are now sinusoidal and equal. The open commutation results in an overshoot in all three phase currents, for both motor **1404** and supply currents **1408**, with the phase A and C currents each reaching peak amplitudes of about 75A in magnitude before subsiding to steady state values.

Associated rotor speed and motor output torque are shown in FIG. 14C and FIG. 14D respectively. The steady state motor speed with a 50Hz supply frequency ($2\pi\times50$Hz = **314**.2rad/s) is **306**.3rad/s due to the motor slip frequency. During the inverter operation, the steady state speed is **305**.6rad/s due to the limited inverter output voltage. As can be seen in FIG. 14D, the motor output torque drops to 0Nm at **1410** during the commutation dead-time. This inherently results in a drop in the rotor speed e.g., at **1412** FIG. 14C. Once the motor is connected to the grid, a transient in both motor speed **1414** and torque **1416** can be seen as (without wanting to be bound by theory, it is theorized that) the motor is effectively experiencing a step input. Both speed and torque settle to their steady state values about 0.08s after connection to the grid.

FIG. 15A is a plot of supply currents, with time, for transition between inverter to grid, according to some embodiments of the disclosure.

FIG. 15B is a plot of motor currents, with time, for transition between inverter to grid, according to some embodiments of the disclosure.

FIG. 15C is a plot of motor speed, with time, for transition between inverter to grid, according to some embodiments of the disclosure.

FIG. 15D is a plot of motor torque, with time, for transition between inverter to grid, according to some embodiments of the disclosure.

When the transition is initiated and once a selected supply voltage sector is entered, first and second phases are connected directly to the supply voltage through the bypass thyristors. The plots illustrate where inverter outputs for the corresponding phases disabled at about the same times as activating the first and second phases through the bypass thyristors. The supply currents can be seen to become sinusoidal for the phases connected via the bypass transistors. After another 0.003s, when a subsequent supply voltage sector is entered, the final phase is connected via the bypass module and disabled through the inverter. Within approximately 0.025s, the currents settle to their steady-state value.

FIG. 16A is a plot of supply currents, with time, for open transition between grid to inverter.

FIG. 16B is a plot of motor currents, with time, for open transition between grid to inverter.

FIG. 16C is a plot of motor torque, with time, for open transition between grid to inverter.

FIG. 16D is a plot of motor speed, with time, for open transition between grid to inverter.

When transitioning from grid to inverter operation, the existing dead-time commutation works as with transition in the opposite direction. However, the thyristors do not deactivate instantaneously. FIG. 16A and FIG. 16B show the supply and motor currents when changing from grid to inverter operation. Once all three phase currents reach 0A, the inverter output is enabled. This result in a transient with the phase currents reaching peak amplitudes of magnitude of about 75A which settle to steady state values at about 0.08s after deactivation gate signals of the bypass module thyristors.

FIG. 16C and FIG. 16D respectively show motor speed and torque for dead-time technique commutation from grid to inverter operation. Motor torque drops to 0Nm **1600** FIG. 16C during the dead-time resulting in a reduction of the rotor speed **1602** FIG. 16D. Once the inverter output is enabled, the motor speed and torque settle to steady state values after a transient.

FIG. 17A is a plot of supply currents, with time, for transition between grid to inverter, according to some embodiments of the disclosure.

FIG. 17B is a plot of motor currents, with time, for transition between grid to inverter, according to some embodiments of the disclosure.

FIG. 17C is a plot of motor torque, with time, for transition between grid to inverter, according to some embodiments of the disclosure.

FIG. 17D is a plot of motor speed, with time, for transition between grid to inverter, according to some embodiments of the disclosure.

If FIG. 17A supply currents drop to zero, for all of the phases, it is theorized, associated with charging of the DC link capacitor/s and low motor currents: DC link capacitor/s may be fully charged during grid operation. Hence, in some embodiments, when power supply is transitions back to inverter operation, the DC link capacitor/s may discharge to briefly supply the load e.g., without drawing current from the grid.

During the transition period, the three phase currents exhibit a transient, initially reaching about 70A magnitude peaks and then dipping to 30A magnitude until settling back to a steady-state value of 40A at 0.08s after disabling of bypass module pathways. Where the motor used in the simulation was a 15kW or higher power rating motor. The transients in the motor currents have an effect on the motor torque and speed as shown in FIG. 17C and FIG. 17D, respectively. The motor torque drops from 100Nm to 30Nm at **1702** FIG. 17C followed by an overshoot, at **1706** FIG. 17C and settles back to the steady state value of about **100**Nm at 0.075s after a start to the commutation sequence. A similar transient occurs in the motor speed, which, at **1704** FIG. 17D, drops from **305**.8rad/s to **303**.2rad/s and then overshoots before settling back to steady state.

**Exemplary implementation**

FIG. 18 is a simplified schematic of an exemplary implementation **1800** of a system, according to some embodiments of the disclosure.

Exemplary system **1800**, in some embodiments, includes a three-phase power supply **1812**, a bypass module **1180**, an inverter drive **1830**, and a load **1860**. Where, in some embodiments, supply **1812** is connected via a miniature circuit breaker (MCB) **1838** enabling connection and disconnection system circuitry to and from supply **1812**. In some embodiments, system **1800** includes one or more fuse modules **1858**, **1840**, **1844** (e.g., for testing purposes) each including fuse holders e.g., a holder for a fuse for each phase e.g., holders carrying high rupturing capacity (HRC) fuses. A fuse holder **1858** is connected to MCB **1838**, e.g., to fuse all three phases. Following fuse module **1858**, a contactor **1828** is placed (for emergency shut down of thyristors and the inverter drive). System **1800** includes, in some embodiments, a braking resistor **1848** e.g., which enables power surge/s (e.g., associated with generation of voltage and/or currents by the motor e.g., associated with active driving loads and/or durations of negative torque produced by the motor) to be dissipated as heat. Where, a braking resistor board (BRB) **1848** allows dissipation energy from the regenerative motor operation **1848** e.g., if the DC link voltage rises above safe levels during transitions. Both inverter drive **1830** and bypass module (thyristor) **1810** outputs are fused **1840**, **1844**, before connecting to an output terminal block (TB) **1842**, which connects the electrical installation to the load **1860**. In some embodiments, load **1860** includes a test rig including an induction motor, a DC motor (providing a variable load to the induction motor) and a torquemeter for the induction motor. In some embodiments, system **1800** includes analog to digital (ADC) circuitry for measurement of the supply voltage e.g., the digital measurement/s being supplied to a controller of inverter **1830**. In some embodiments, the ADC circuitry is hosted by an inverter module or component.

In the exemplary embodiment, frequency control uses PLLs (e.g., as opposed to calculation e.g., via trigonometric function) for inverter output and supply voltages. A potential benefit being increased speed.

In some embodiments, the system includes isolation of inverter electronics from the bypass module, for example, to provide isolation of the inverter from the grid voltages passing through the bypass module. Where, in some embodiments, isolation is provided by driving circuitry between the bypass module and the inverter e.g., by a DC/DC converter and/or optocoupler between the inverter controller control signal and the gates of each thyristor pair switch. In some embodiments, driving circuitry for the bypass module switches one or more additional component e.g., for decoupling and/or noise filtering and/or to provide access for measurement.

FIGs. 19A-C are plots of motor torque with time, for inverter to grid transitions, according to some embodiments of the disclosure.

FIG. 19A shows a plot of motor torque with time for inverter to grid transition where the inverter uses SPWM .

FIG. 19B shows a plot of motor torque with time for inverter to grid transition with a 3$^{rd}$ harmonic compensation using the DC link mid-point voltage (e.g., an instantaneous value thereof). Where this voltage is measured and/or determined from measurements e.g., of the DC link mid-voltage e.g., at node **854**. Where measurements of the DC link mid-voltage are used, delay introduced by ADC conversion (e.g., by low pass filter/s of ADC/s) of the measurement are taken into account.

FIG. 19C shows a plot of motor torque with time for inverter to grid transition without a 3$^{rd}$ harmonic injection, where the neutral cable is connected directly to the DC midpoint. A potential benefit of which is a smoother transition as the inverter output voltage more closely mirrors that of the grid.

**General**

As used within this document, the term “about” refers to±20%

The terms “comprises”, “comprising”, “includes”, “including”, “having” and their conjugates mean “including but not limited to”.

The term “consisting of” means “including and limited to”.

As used herein, singular forms, for example, “a”, “an” and “the” include plural references unless the context clearly dictates otherwise.

Within this application, various quantifications and/or expressions may include use of ranges. Range format should not be construed as an inflexible limitation on the scope of the present disclosure. Accordingly, descriptions including ranges should be considered to have specifically disclosed all the possible subranges as well as individual numerical values within that range. For example, description of a range such as from 1 to 6 should be considered to have specifically disclosed subranges such as from 1 to 3, from 1 to 4, from 1 to 5, from 2 to 4, from 2 to 6, from 3 to 6 etc., as well as individual numbers within the stated range and/or subrange, for example, 1, 2, 3, 4, 5, and 6. Whenever a numerical range is indicated within this document, it is meant to include any cited numeral (fractional or integral) within the indicated range.

It is appreciated that certain features which are (e.g., for clarity) described in the context of separate embodiments, may also be provided in combination in a single embodiment. Where various features of the present disclosure, which are (e.g., for brevity) described in a context of a single embodiment, may also be provided separately or in any suitable sub-combination or may be suitable for use with any other described embodiment. Features described in the context of various embodiments are not to be considered essential features of those embodiments, unless the embodiment is inoperative without those elements.

Although the present disclosure has been described in conjunction with specific embodiments thereof, it is evident that many alternatives, modifications, and variations will be apparent to those skilled in the art. Accordingly, this application intends to embrace all such alternatives, modifications and variations that fall within the spirit and broad scope of the appended claims.

All references (e.g., publications, patents, patent applications) mentioned in this specification are herein incorporated in their entirety by reference into the specification, e.g., as if each individual publication, patent, or patent application was individually indicated to be incorporated herein by reference. Citation or identification of any reference in this application should not be construed as an admission that such reference is available as prior art to the present disclosure. In addition, any priority document(s) and/or documents related to this application (e.g., co-filed) are hereby incorporated herein by reference in its/their entirety.

Where section headings are used in this document, they should not be interpreted as necessarily limiting.

**CLAIMS:**

1. A method of transitioning between supplying electrical power from a three phased supply to a load through three activated electrical supply pathways of a first supply module, to supplying power to the load through three activated electrical supply paths of a second supply module, comprising:

monitoring a sector of said three phase supply;

selecting a first phase for transition, based on said sector; and

activating a first pathway through said second supply module, corresponding to said first phase and deactivating a first pathway through said first supply module corresponding to said first phase, while at least one pathway of said first supply module remains activated.

2. The method according to claim 1, comprising selecting a second phase for transition, based on said sector;

activating a second pathway through said second supply module, corresponding to said second phase and deactivating a second pathway through said first supply module corresponding to said second phase.

3. The method according to claim 2, comprising selecting a third phase for transition, based on said sector;

activating a third pathway through said second supply module, corresponding to said third phase and deactivating a third pathway through said first supply module corresponding to said third phase.

4. The method according to any one of claims 2-3, wherein said selecting, said activating, and said deactivating for said first phase and said second phase are performed during a same power supply sector.

5. The method according to any one of claims 4, wherein, after a time delay corresponding to a sector duration, said activating, and said deactivating for said third phase is performed.

6. The method according to any one of claims 2-3, wherein said selecting, said activating, and said deactivating for said first phase and said second phase are performed during a same power supply sector.

7. The method according to claim 6, wherein said selecting, said activating, and said deactivating for said first phase is performed in a first power supply sector;

wherein said selecting, said activating, and said deactivating for said second phase and said third phase is performed in a first power supply sector.

8. The method according to any one of claims 1-7, wherein said deactivating occurs after said activating.

9. The method according to any one of claims 1-8, wherein said first power supply module is an inverter, and wherein said second power supply module is a bypass module configured to deliver said power supply to said load.

10. The method according to claim 9, wherein said inverter is a switched mode variable frequency power supply receiving three phase power from a grid supply.

11. The method according to claim 3, wherein said deactivating for each of said first, second, and third phases is prior to said activating for each of said first, second, and third phases;

wherein said activating for each of said first, second, and third phases is performed in a different sector of said three phase supply.

12. The method according to claim 11, wherein said second power supply module is an inverter, and wherein said first power supply module is a bypass module configured to deliver said power supply to said load.

13. The method according to claim 12, wherein said inverter is a switched mode variable frequency power supply receiving three phase power from a grid supply.

14. The method according to any one of claims 11-13, wherein said activating for one or more of said first, second, and third phases is upon verifying said deactivating.

15. The method according to claim 14, wherein said verifying comprises verifying that a measurement of current through a deactivated pathway is below a threshold.

16. The method according to claim 15, wherein said verifying comprises receiving a measurement of said current through said deactivated pathway.

17. A power supply system comprising:

a variable speed drive (VSD) configured to receive a three phase power supply and to deliver a variable frequency three phased power supply to a load through a plurality of VSD electrical pathways;

a bypass module configured to receive and deliver said three phased power supply to said load through a plurality of bypass electrical pathways;

a controller configured to control transition between supplying said load through said VSD and through said bypass module by generating control signals for activation and deactivation of said plurality of VSD electrical pathways and said plurality of bypass electrical pathways, which controller configured to:

identify a phase state of said three phase power supply;

select a first phase for transition, based on said phase state; and

activate a first bypass pathway and deactivate a first VSD pathway, while at least one VSD pathway remains activated; **or**

activate a first VSD pathway and deactivate a first bypass pathway, while at least one bypass pathway remains activated.

18. A controller for a power supply system comprising a variable speed drive (VSD) configured to receive a three phase power supply and to deliver a variable frequency three phased power supply to a load through a plurality of VSD electrical pathways and a bypass module configured to receive and deliver said three phased power supply to said load through a plurality of bypass electrical pathways, the controller configured to:

control transition between supplying said load through said VSD and through said bypass module by generating control signals for activation and deactivation of said plurality of VSD electrical pathways and said plurality of bypass electrical pathways, which controller configured to:

identify a phase state of said three phase power supply;

select a first phase for transition, based on said phase state; and

activate a first bypass pathway and deactivate a first VSD pathway, while at least one VSD pathway remains activated; **or**

activate a first VSD pathway and deactivate a first bypass pathway while at least one bypass pathway remains activated.

19. A controller configured to generate switching signals for commutation between a variable frequency drive (VFD) and a bypass module each connecting a three phase alternating current (AC) power supply to a load, where each of said VFD and said bypass module have first, second, and third, pathways respectively corresponding to first, second, and third phases of said power supply, the controller configured to:

monitor a sector of said three phase AC power supply;

activate, based on said sector, during said sector one or two pathways through said bypass module, and disconnect, during said sector, a corresponding one or two pathways through said VFD;

activate, in a subsequent sector, a remaining one or two pathways through said bypass module and disconnect, during said subsequent sector, a corresponding remaining one or two pathways through said VFD.

20. The controller according to claim 19, wherein the controller is configured to disconnect said corresponding one or two pathways through said VFD after the one or two pathways through said bypass module have been activated.

21. The controller according to any one of claims 19-20, wherein the controller is configured to disconnect said remaining one or two pathways through said VFD after the one or two remaining pathways through said bypass module have been activated.

22. The controller according to any one of claims 19-21, wherein said controller is configured to verify that a voltage vector of power supplied to said load through said VFD is sufficiently aligned with a voltage vector of said power supply.

23. A controller configured to generate switching signals for commutation between a variable frequency drive (VFD) and a bypass module each connecting a three phase alternating current (AC) power supply to a load, where each of said VFD and said bypass module have first, second, and third, pathways respectively corresponding to first, second, and third phases of said power supply, the controller configured to:

monitor a sector of said three phase AC power supply;

deactivate, based on said sector, a first pathway through said bypass module, and activate, once said first pathway is deactivated, a corresponding first pathway through said VFD.

24. The controller according to claim 23, wherein said controller is configured to deactivate a second pathway through said bypass module, and activate, once said second pathway is deactivated, during a subsequent sector, a corresponding second pathway through said VFD.

25. The controller according to claim 24, wherein said controller is configured to deactivate a third pathway through said bypass module, and activate, once said third pathway is deactivated, during a sector following said subsequent sector, a corresponding third pathway through said VFD.

26. A controller configured to generate switching signals for a variable frequency drive (VFD) and a bypass module connecting a three phase alternating current (AC) power supply to a motor, the controller configured to:

monitor phase timing of said AC power supply;

switch between power supply to said motor through said VFD and power supply to said motor through said bypass module while continuously supplying power to said motor by, based on said phase timing, enabling current paths corresponding to less than all phases of said AC power supply through both said bypass module and said VFD.

27. A commutation method comprising:

controlling frequency of three phase power supplied through a variable frequency drive (VFD), to a load, to match the frequency and phase of load consumption to the frequency and phase of a three phase grid supply;

maintaining timing of control signals to said VFD;

monitoring a sector of said three phase supply;

selecting a first phase for transition, based on said sector;

activating, over at least two sectors of a frequency of the grid, pathways through a bypass module, and deactivating pathways through the VFD, while maintaining at least one active pathway;

deactivating, over at least two sectors of a frequency of the grid, pathways through a bypass module, and activating pathways through the VFD, while maintaining at least one active pathway, using said timing of said control signals to said VFD.

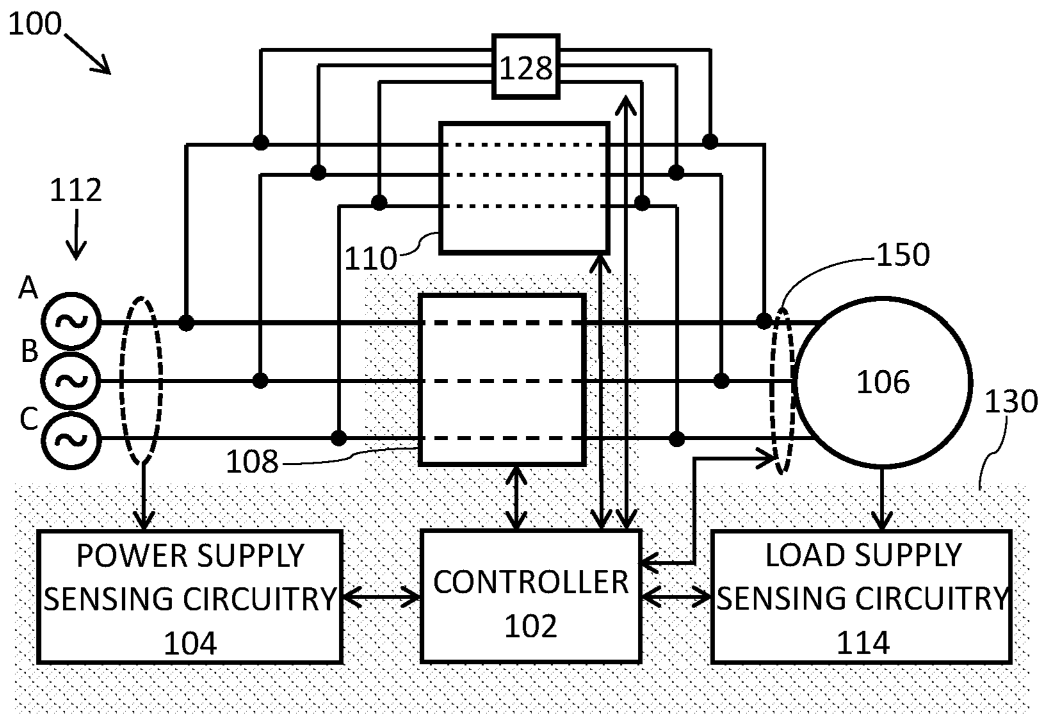

100
112
A
B
C
128
110
150
108
106
130
POWER SUPPLY SENSING CIRCUITRY 104
CONTROLLER 102
LOAD SUPPLY SENSING CIRCUITRY 114

*FIG. 1*

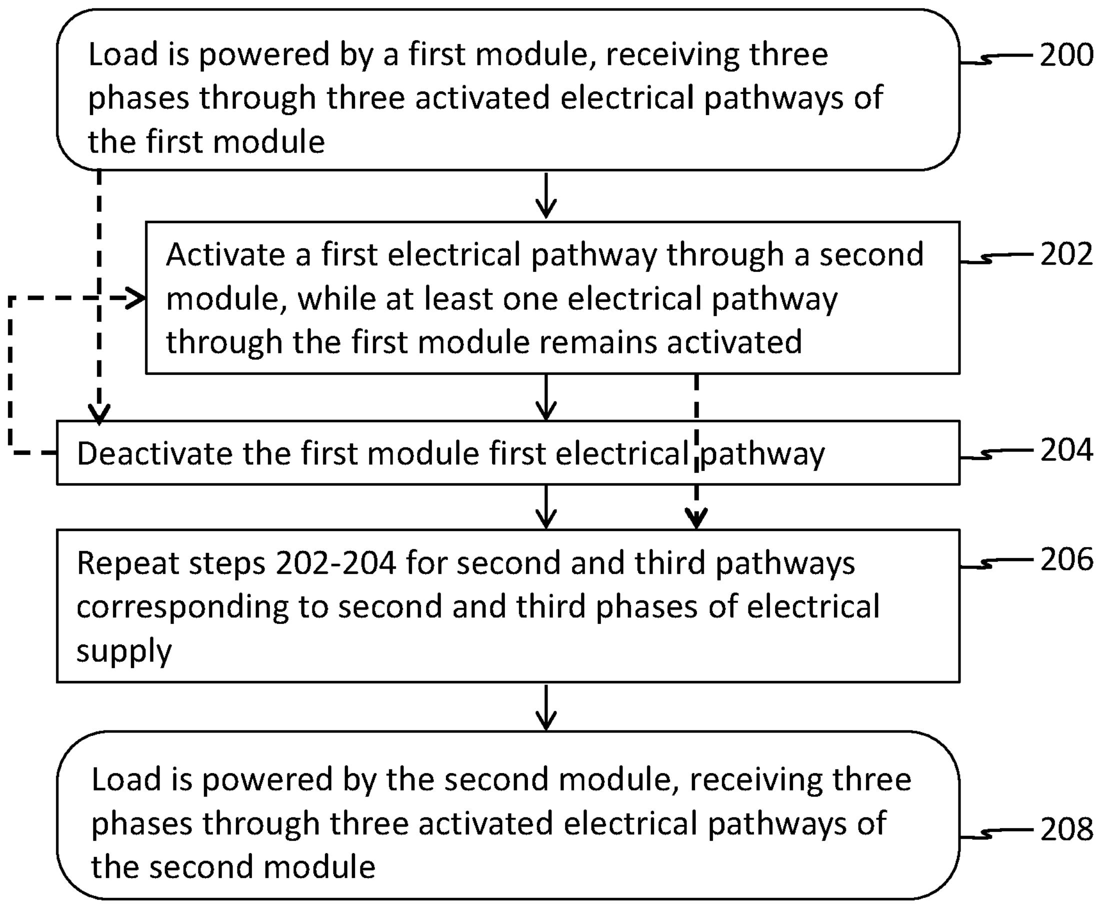

Load is powered by a first module, receiving three phases through three activated electrical pathways of the first module
200
Activate a first electrical pathway through a second module, while at least one electrical pathway through the first module remains activated
202
Deactivate the first module first electrical pathway
204
Repeat steps 202-204 for second and third pathways corresponding to second and third phases of electrical supply
206
Load is powered by the second module, receiving three phases through three activated electrical pathways of the second module
208

*FIG. 2*

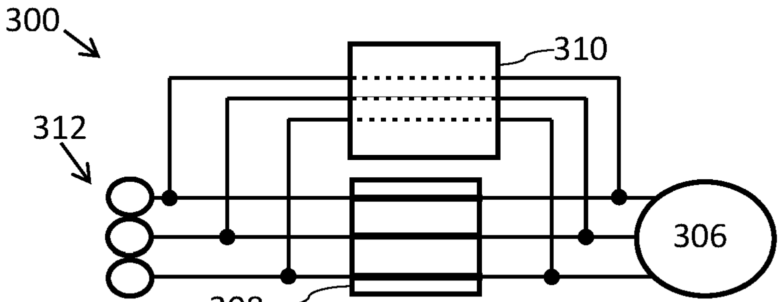



FIG. 3A

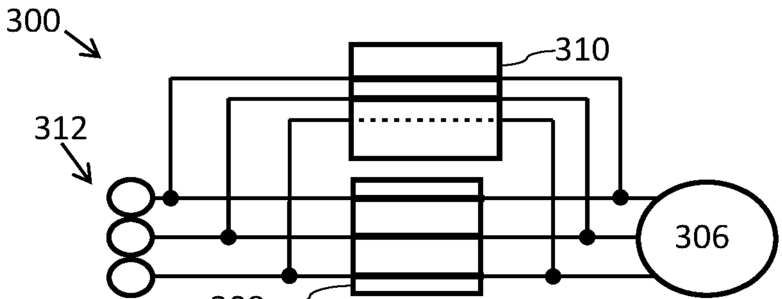



FIG. 3B

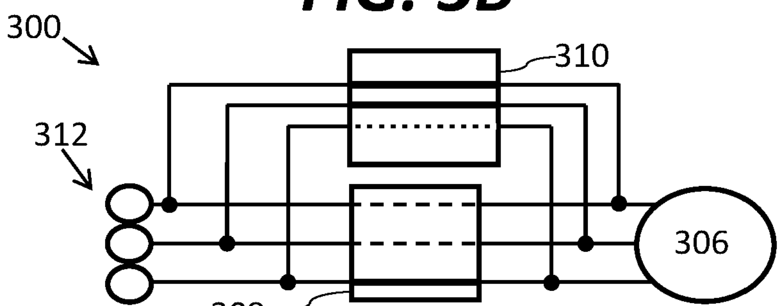



FIG. 3C

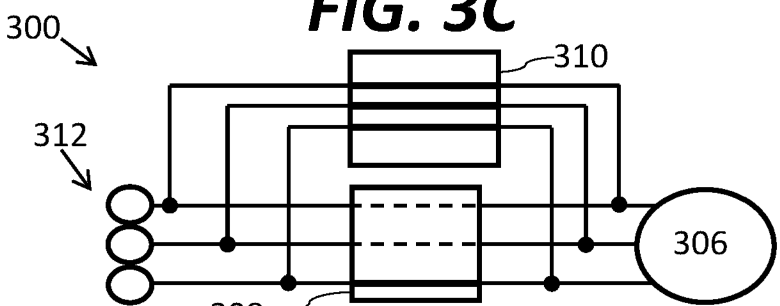



FIG. 3D

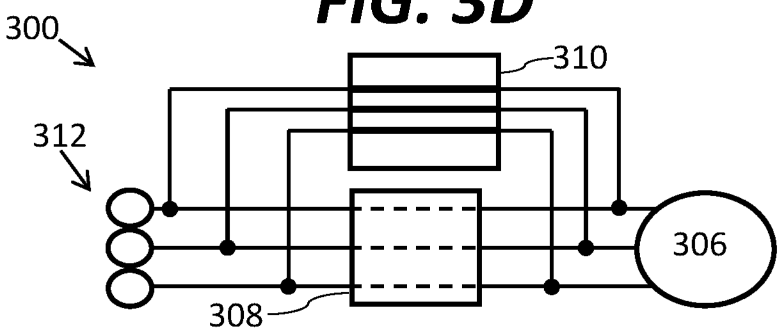



FIG. 3E

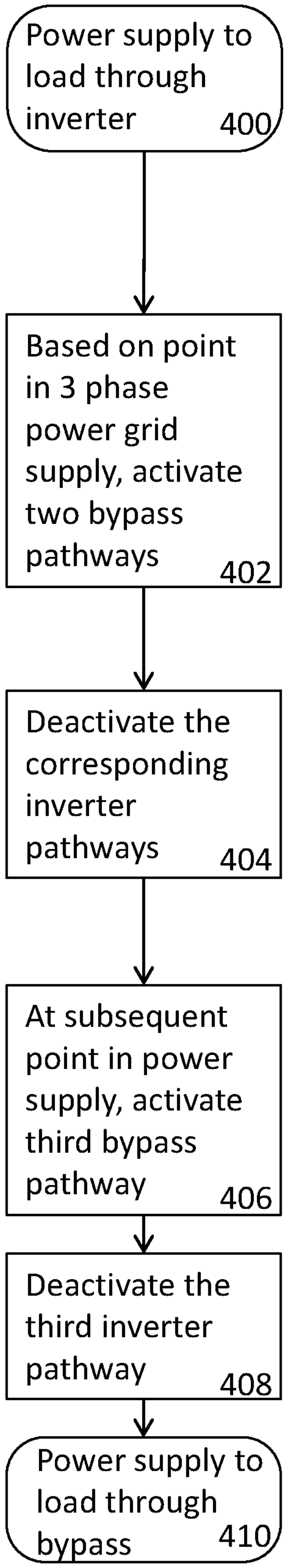



FIG. 4

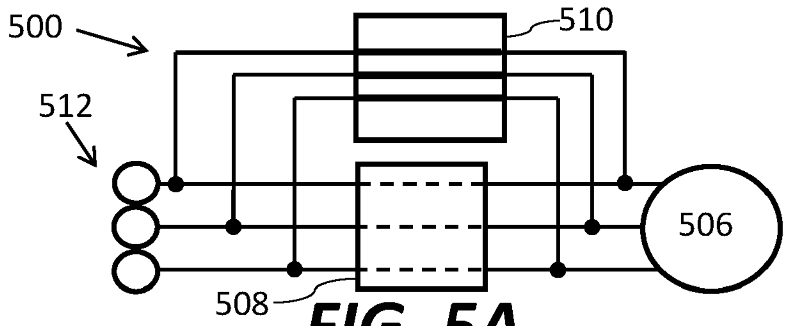



FIG. 5A

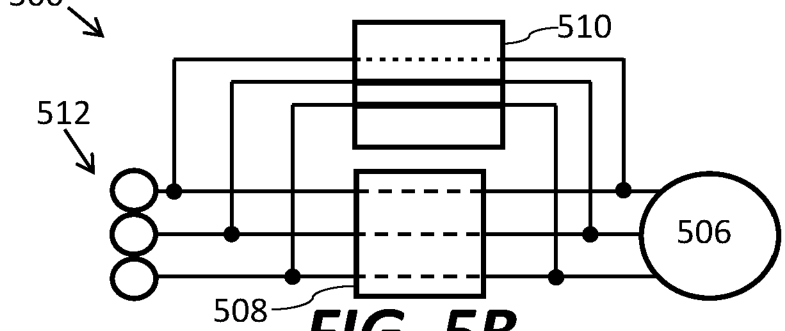



FIG. 5B

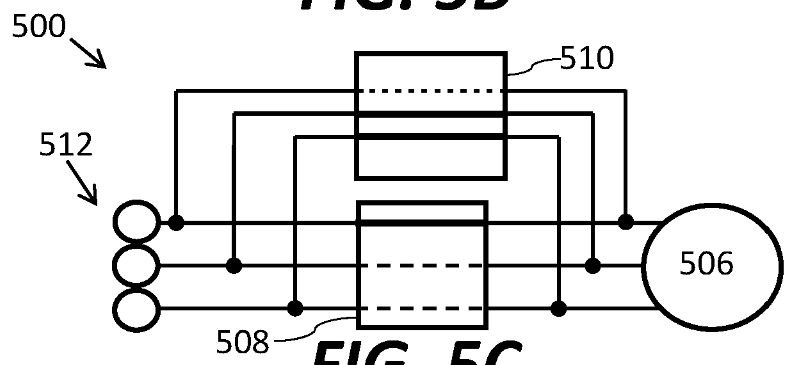



FIG. 5C

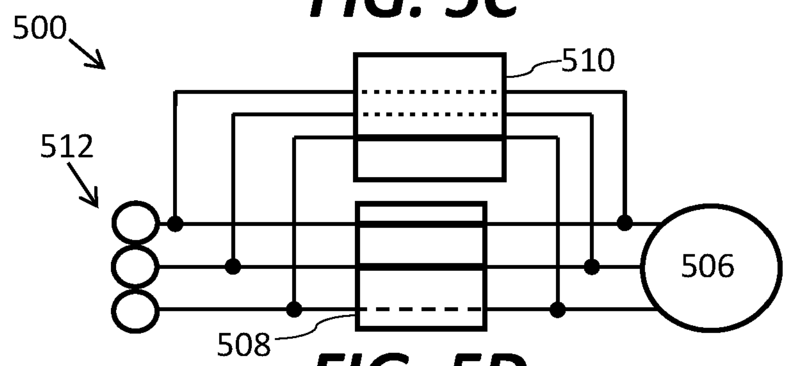



FIG. 5D

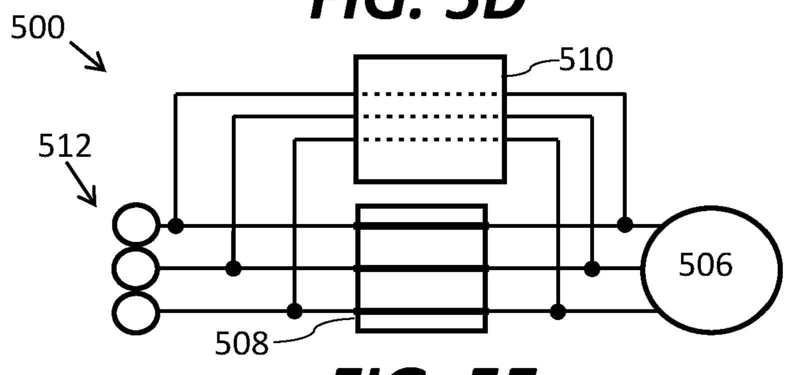



FIG. 5E

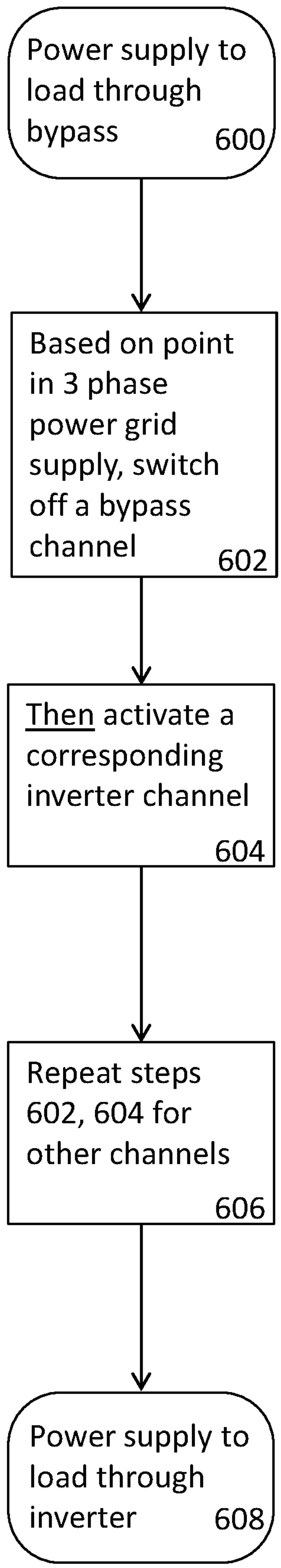
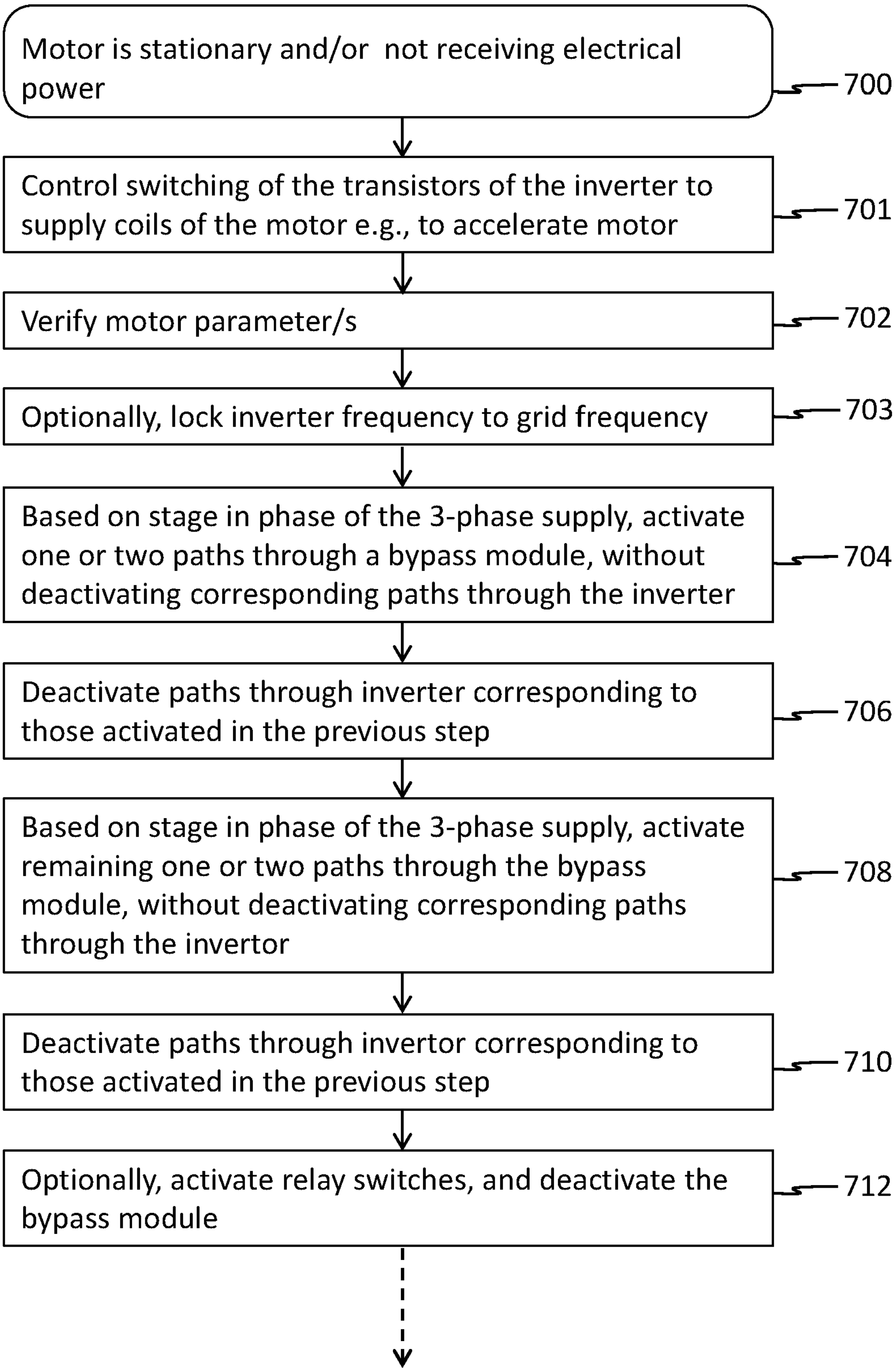



FIG. 6



Motor is stationary and/or not receiving electrical power
700
Control switching of the transistors of the inverter to supply coils of the motor e.g., to accelerate motor
701
Verify motor parameter/s
702
Optionally, lock inverter frequency to grid frequency
703
Based on stage in phase of the 3-phase supply, activate one or two paths through a bypass module, without deactivating corresponding paths through the inverter
704
Deactivate paths through inverter corresponding to those activated in the previous step
706
Based on stage in phase of the 3-phase supply, activate remaining one or two paths through the bypass module, without deactivating corresponding paths through the invertor
708
Deactivate paths through invertor corresponding to those activated in the previous step
710
Optionally, activate relay switches, and deactivate the bypass module
712


FIG. 7A

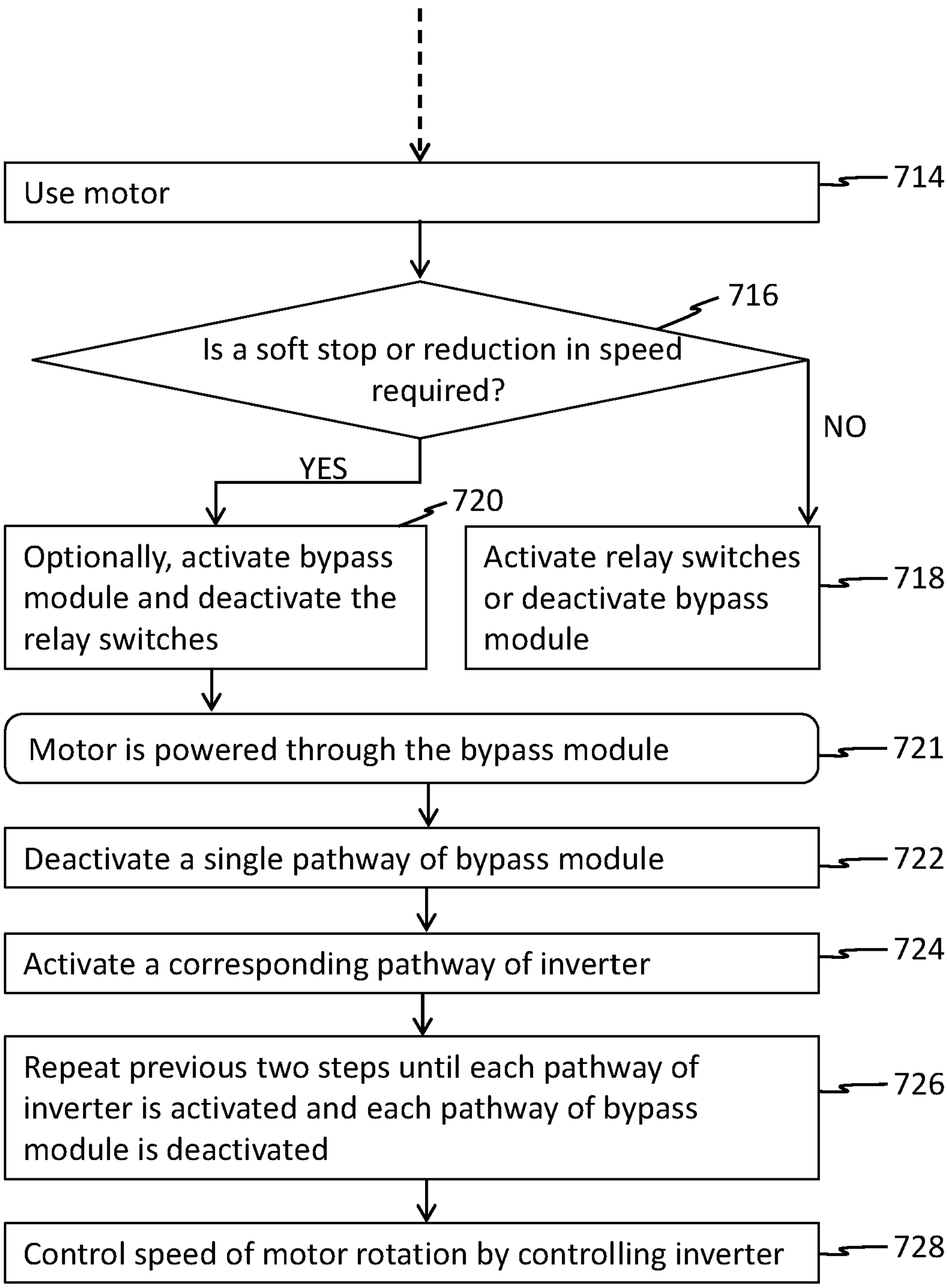

Use motor
714
Is a soft stop or reduction in speed required?
716
YES
NO
720
Optionally, activate bypass module and deactivate the relay switches
Activate relay switches or deactivate bypass module
718
Motor is powered through the bypass module
721
Deactivate a single pathway of bypass module
722
Activate a corresponding pathway of inverter
724
Repeat previous two steps until each pathway of inverter is activated and each pathway of bypass module is deactivated
726
Control speed of motor rotation by controlling inverter
728

*FIG. 7B*

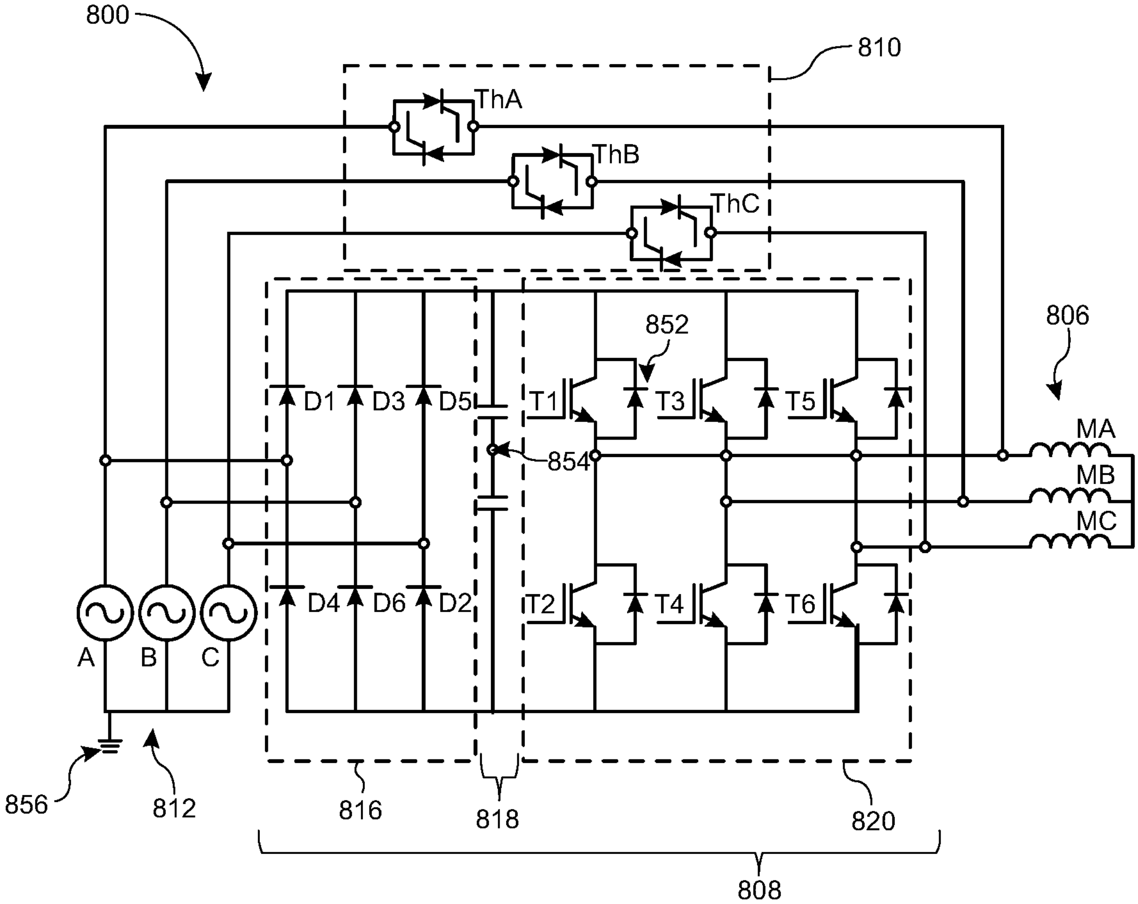

800
810
ThA
ThB
ThC
852
806
D1
D3
D5
T1
T3
T5
MA
854
MB
MC
D4
D6
D2
T2
T4
T6
A
B
C
856
812
816
818
820
808

FIG. 8A

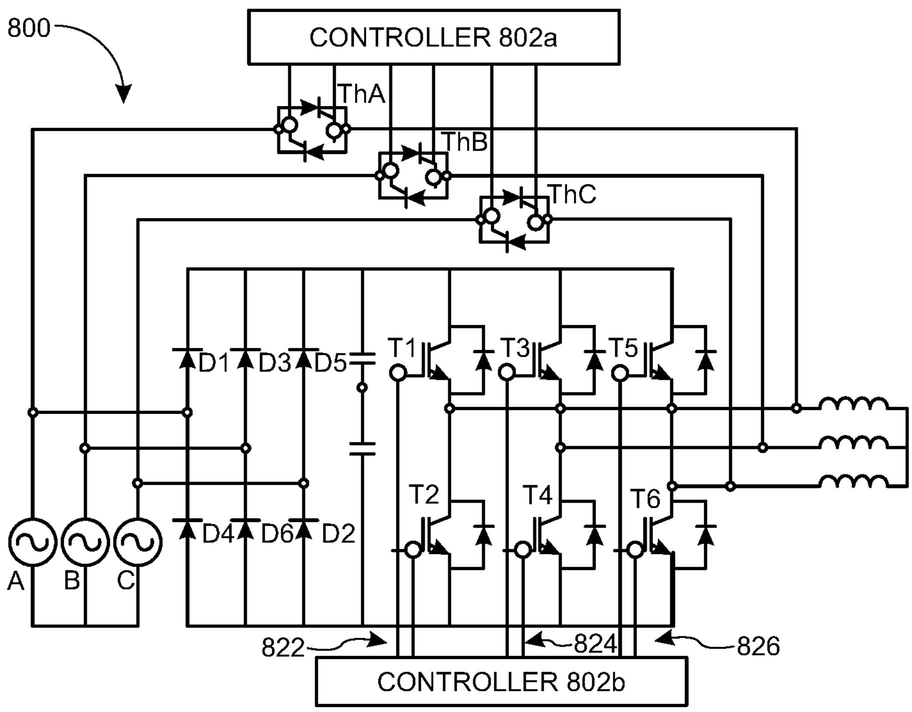

800
CONTROLLER 802a
ThA
ThB
ThC
D1
D3
D5
T1
T3
T5
T2
T4
T6
D4
D6
D2
A
B
C
822
824
826
CONTROLLER 802b

FIG. 8B

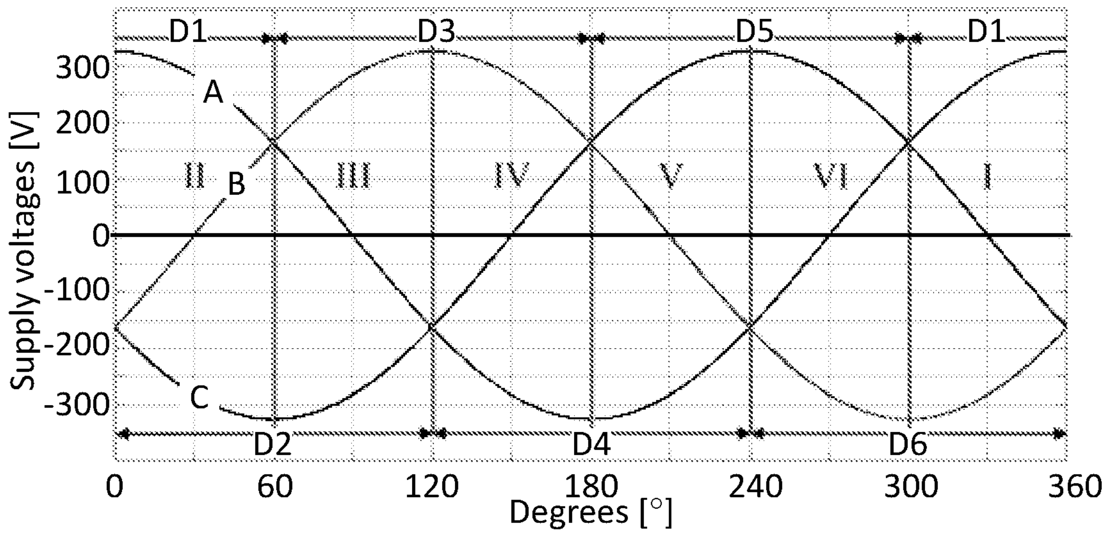

D1
D3
D5
D1
A
B
C
II
III
IV
V
VI
I
D2
D4
D6
Supply voltages [V]
300
200
100
0
-100
-200
-300
0
60
120
180
240
300
360
Degrees [°]

*FIG. 9*

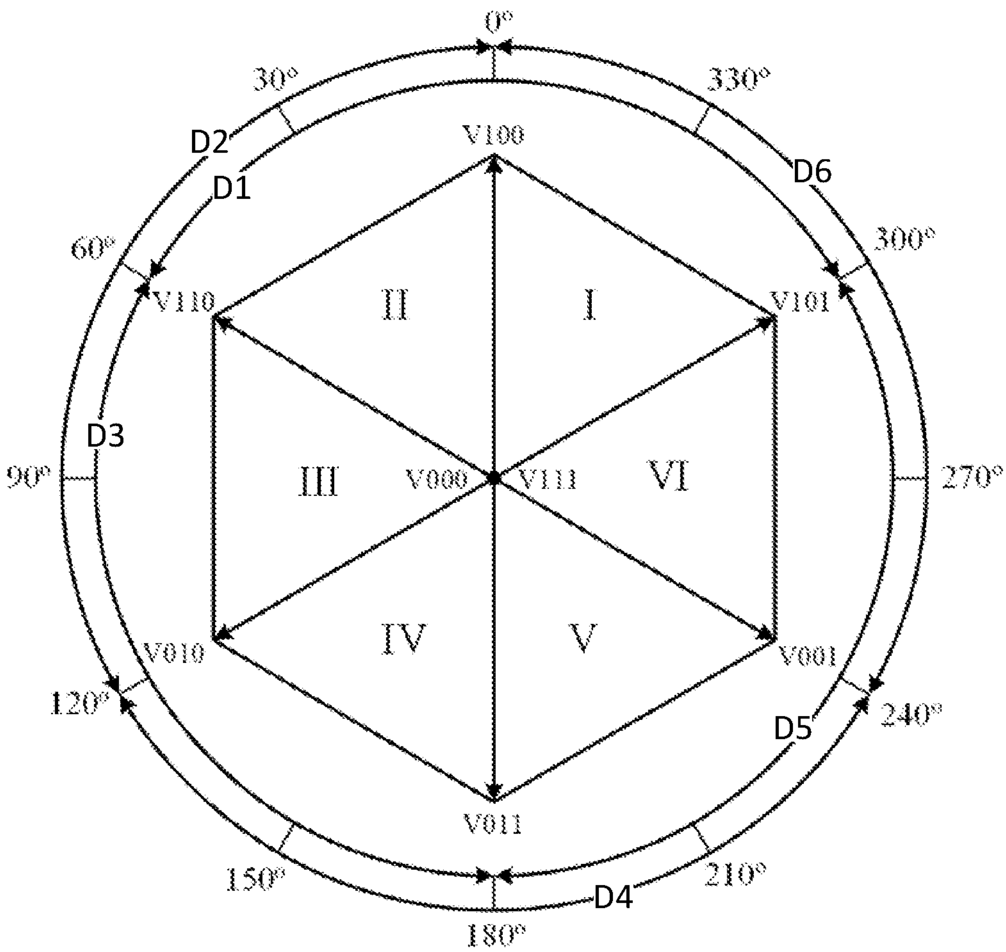

0°
30°
330°
60°
300°
90°
270°
120°
240°
150°
210°
180°
D1
D2
D3
D4
D5
D6
V100
V110
V101
V010
V001
V011
V000
V111
I
II
III
IV
V
VI

*FIG. 10*

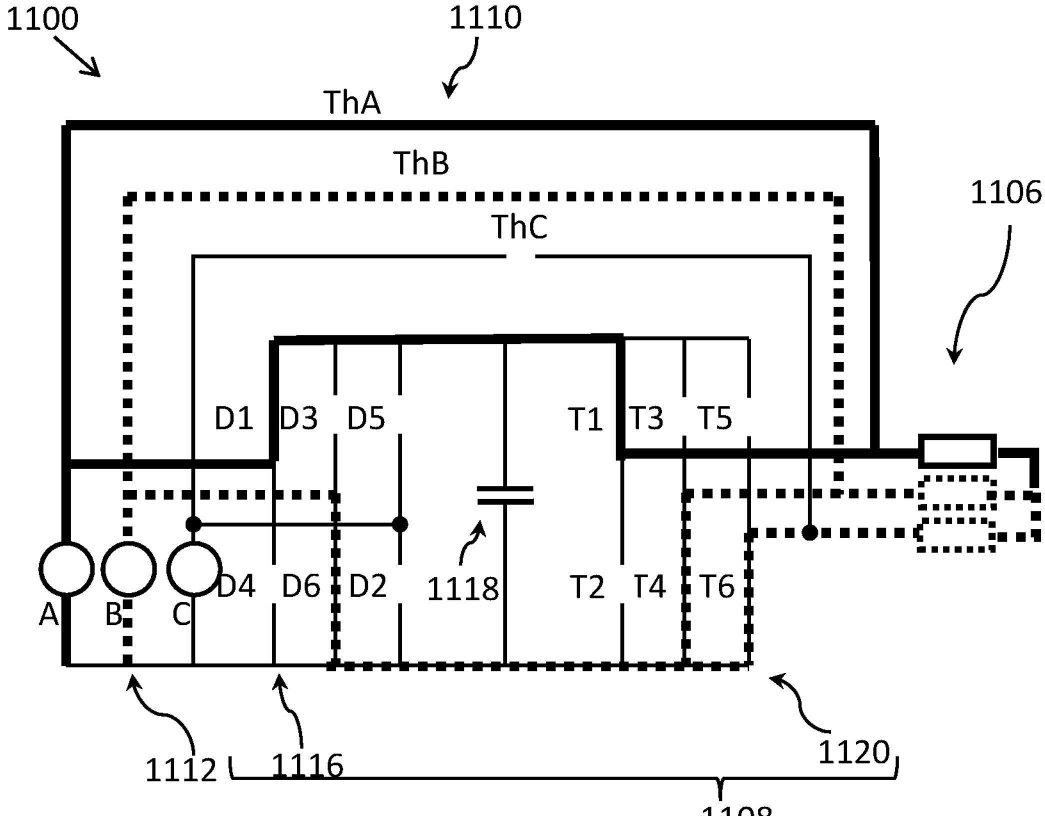



FIG. 11A

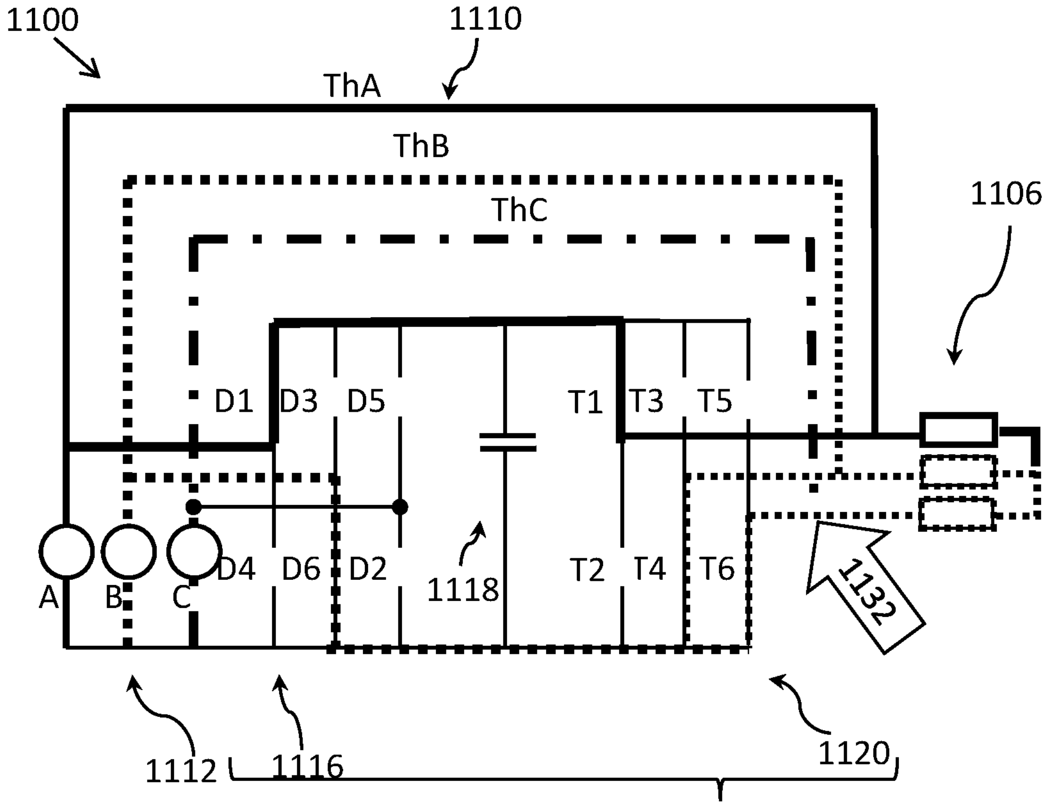



FIG. 11B

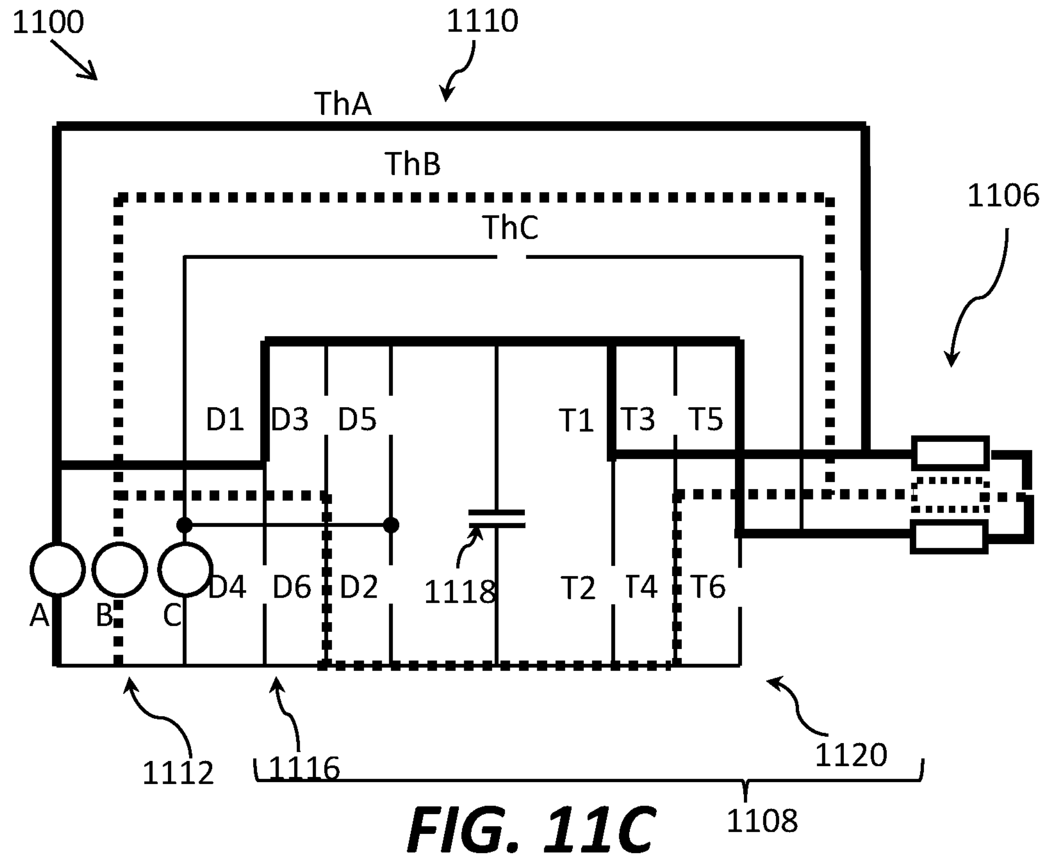



FIG. 11C

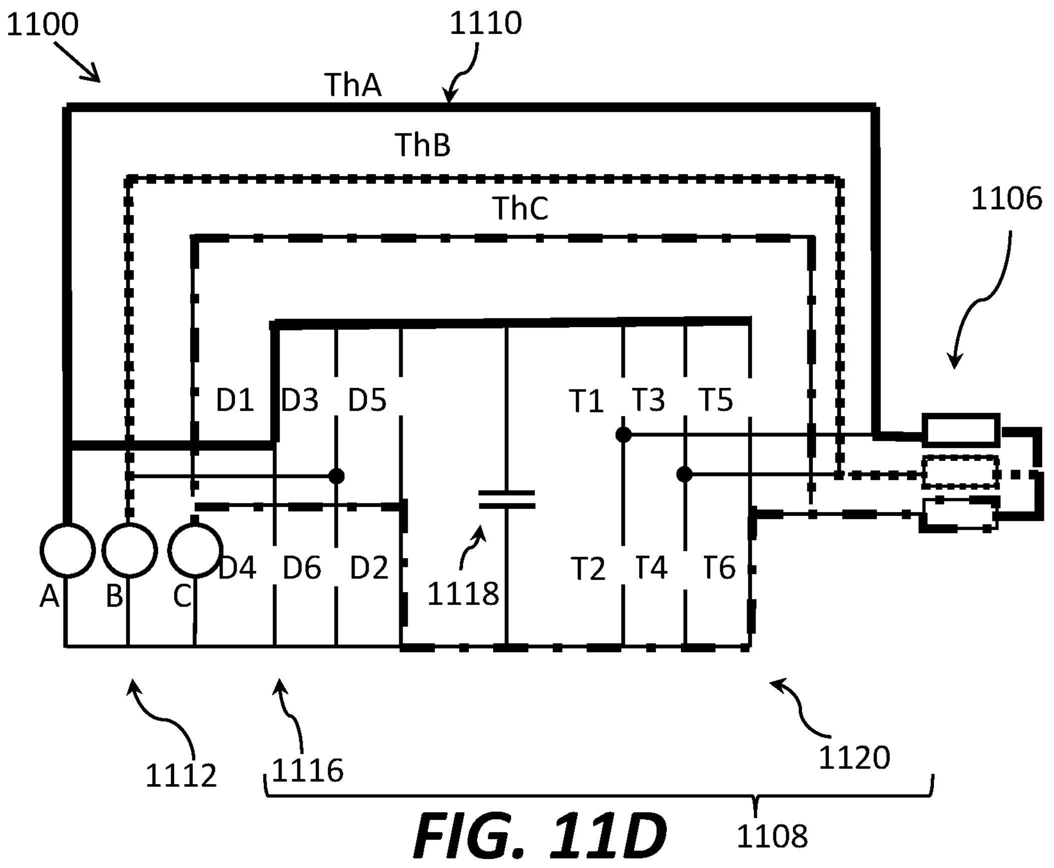



FIG. 11D

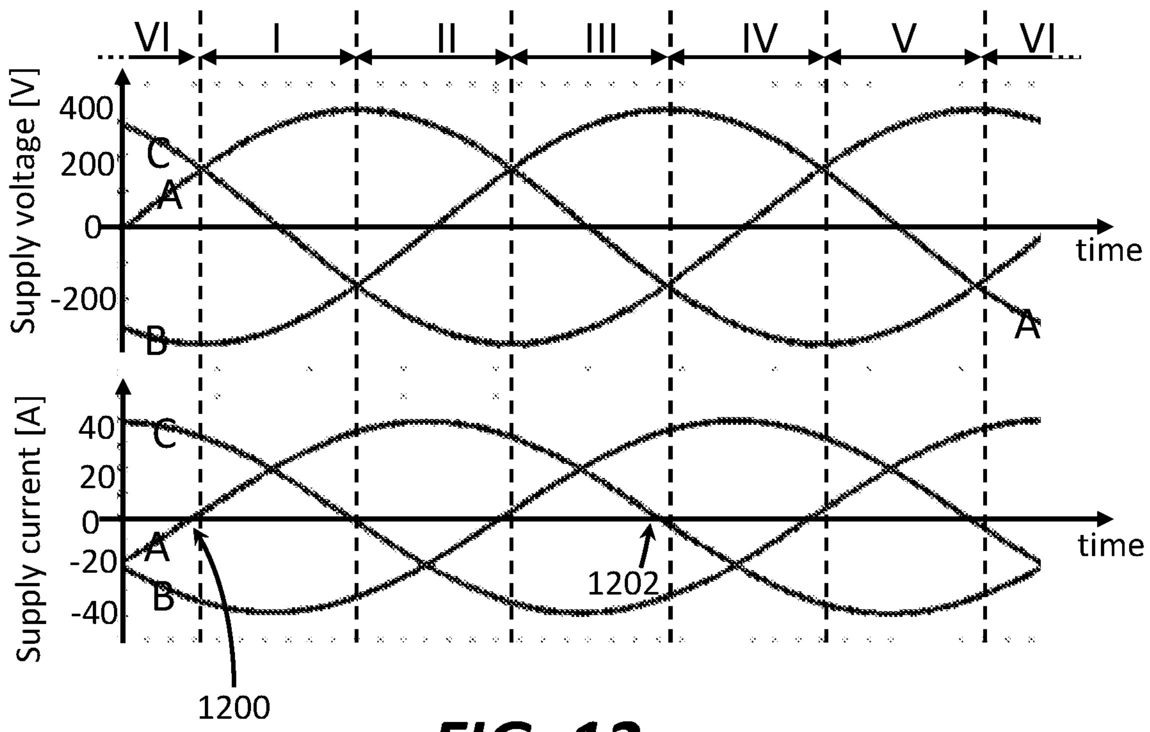



FIG. 12

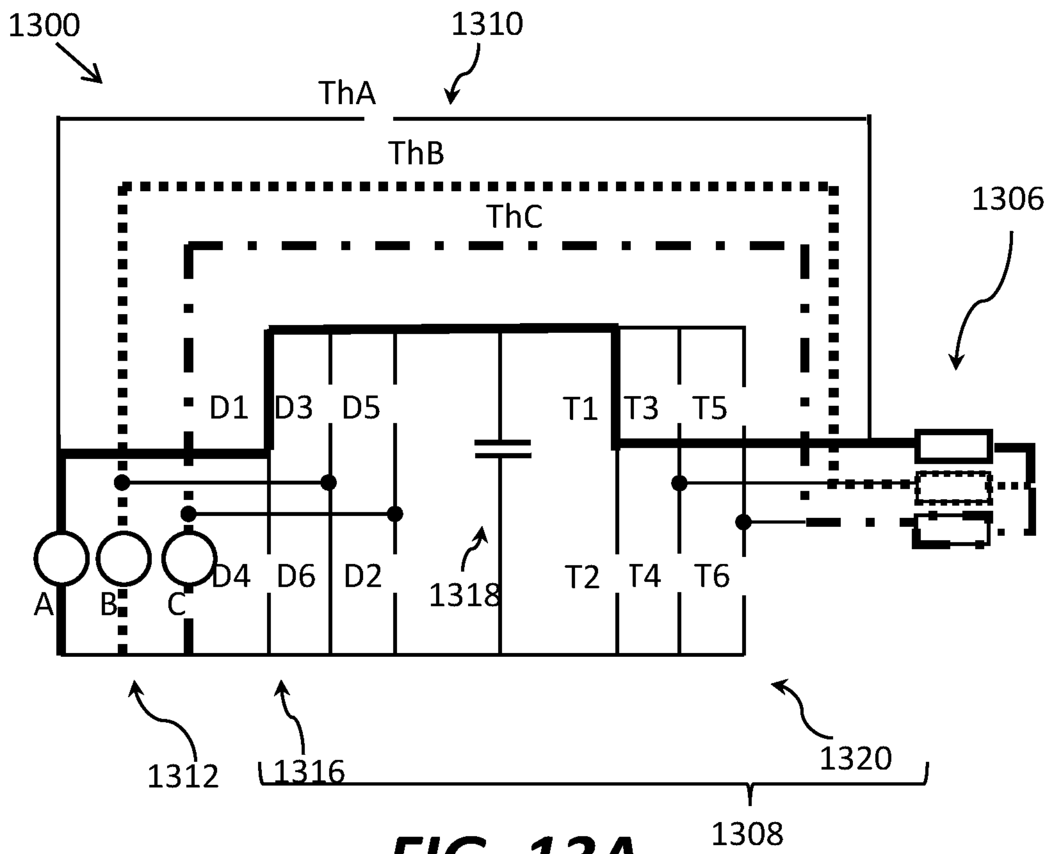



FIG. 13A

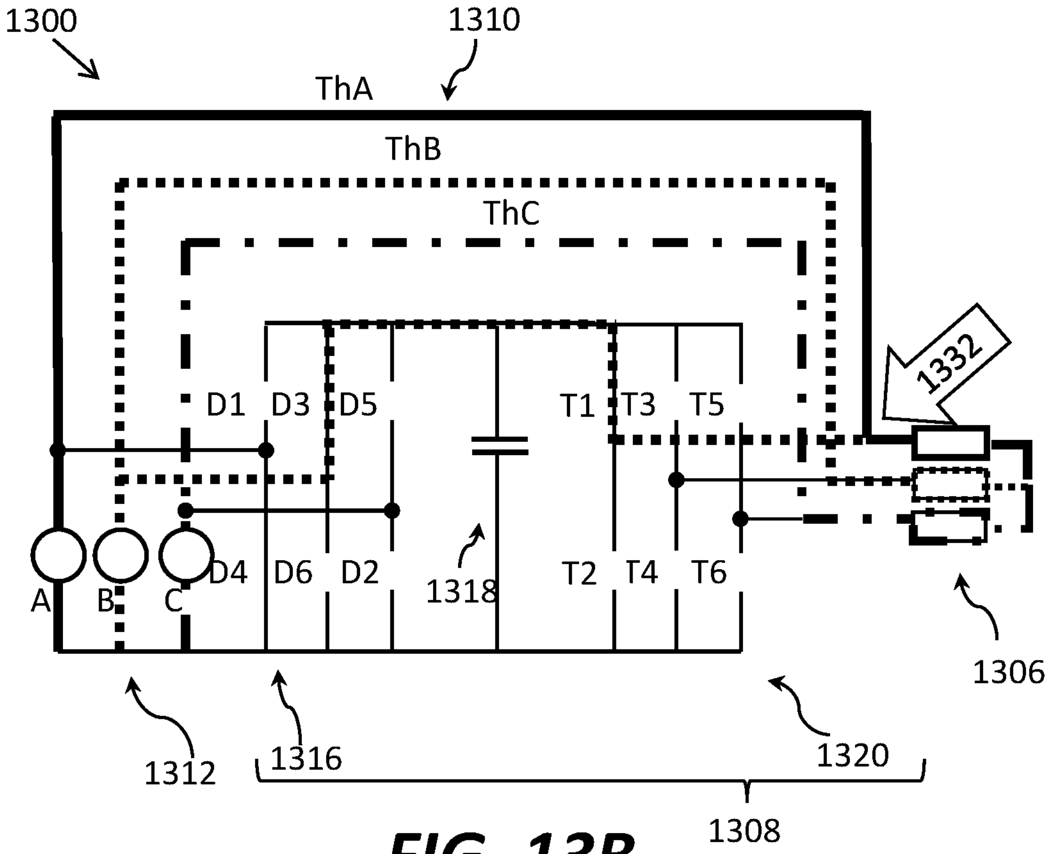



FIG. 13B

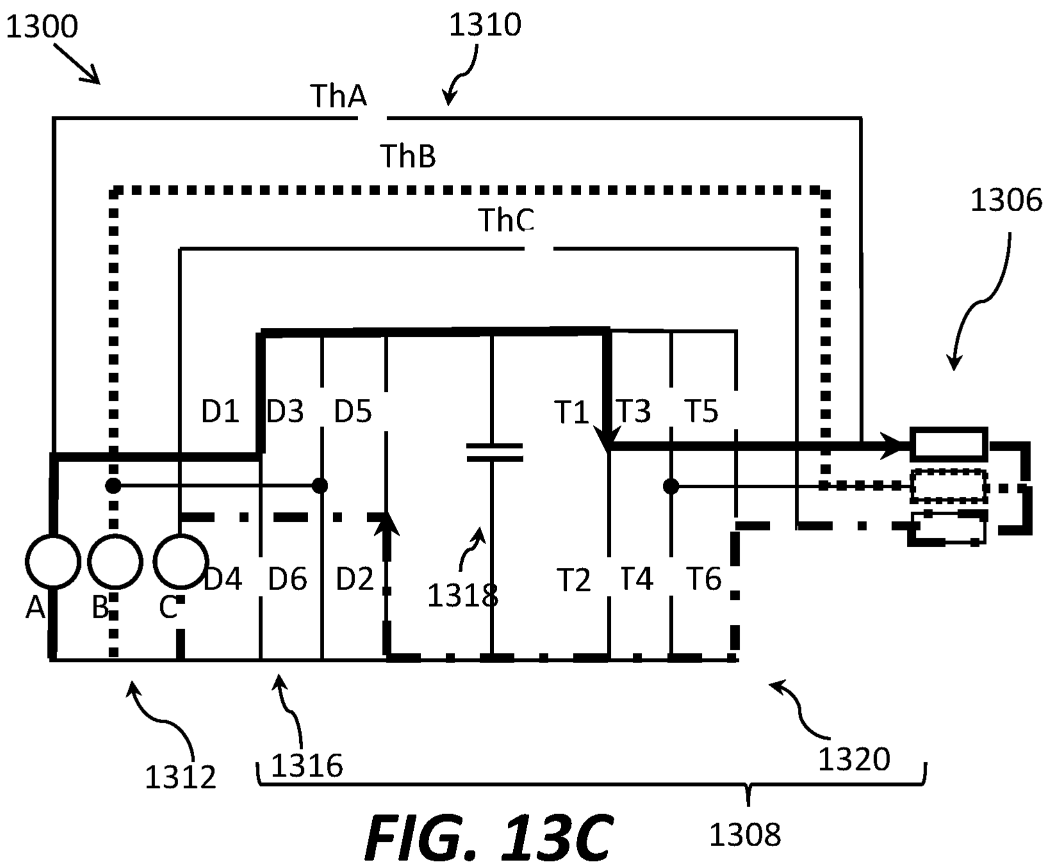



FIG. 13C

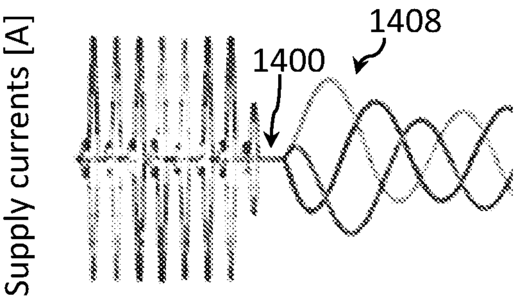



FIG. 14A

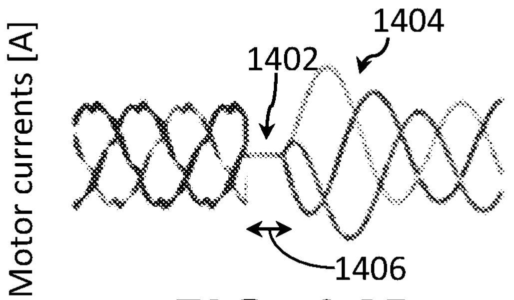



FIG. 14B

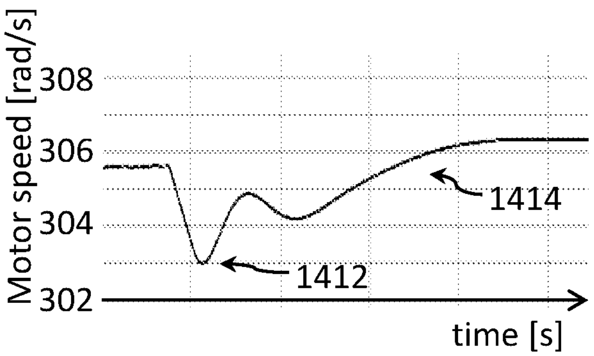



FIG. 14C

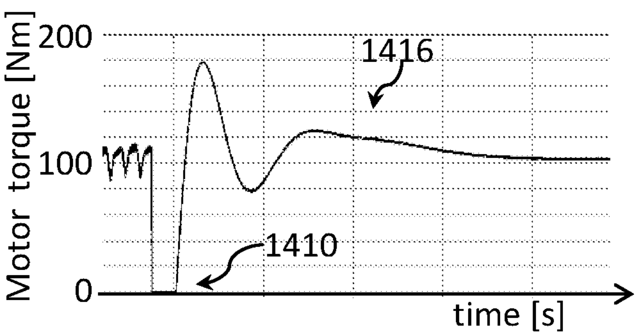



FIG. 14D

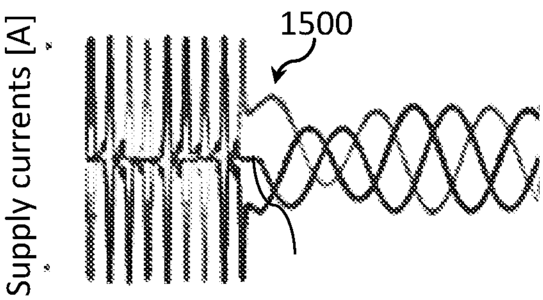



FIG. 15A

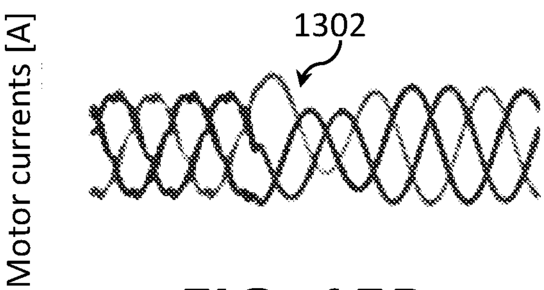



FIG. 15B

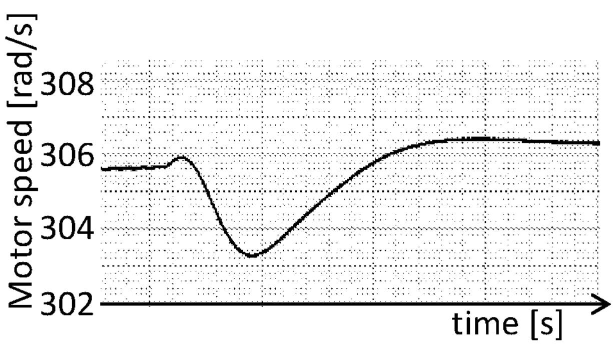



FIG. 15C

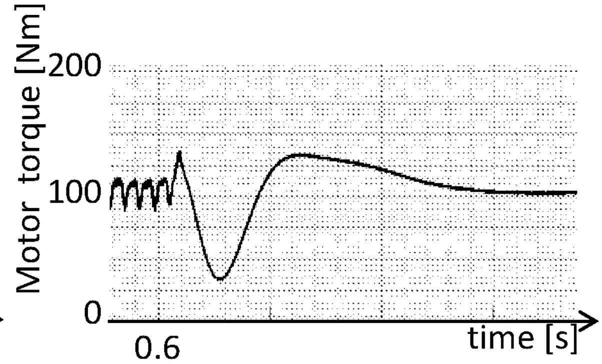



FIG. 15D

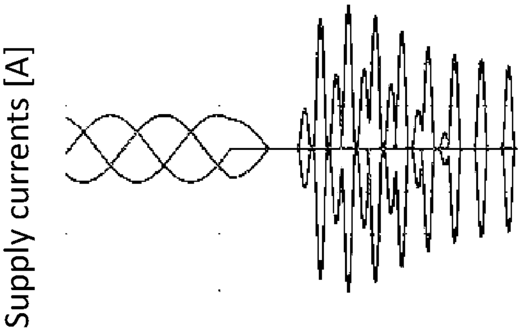



FIG. 16A

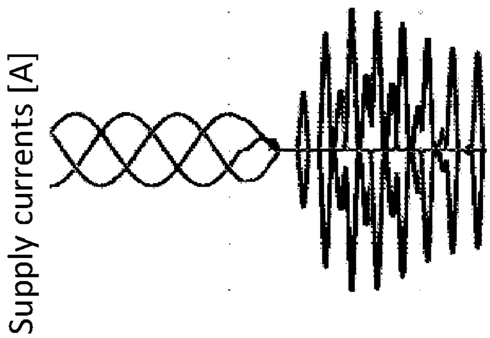



FIG. 17A

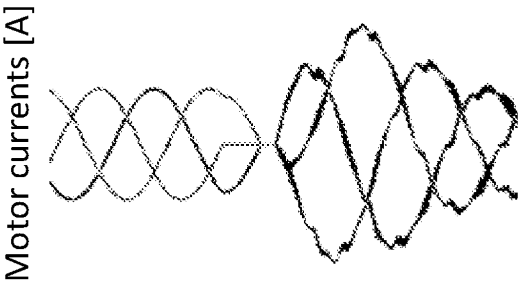



FIG. 16B

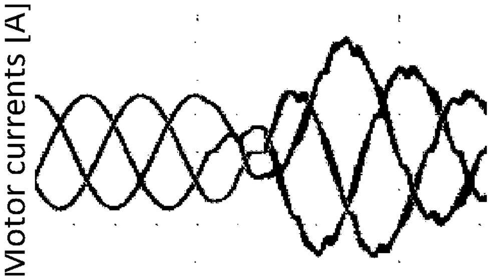



FIG. 17B

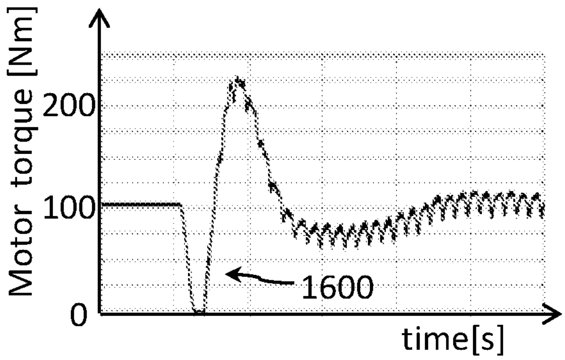



FIG. 16C

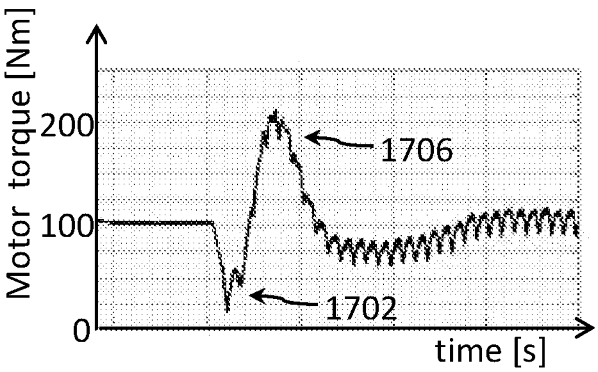



FIG. 17C

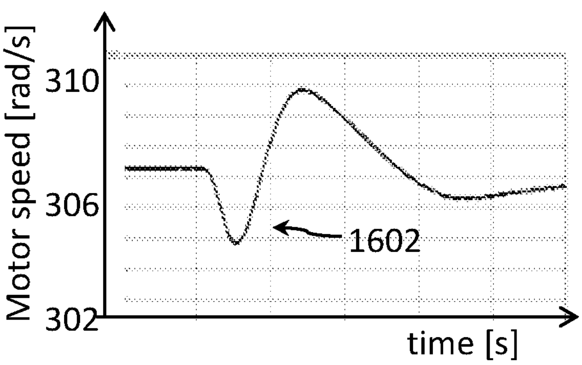



FIG. 16D

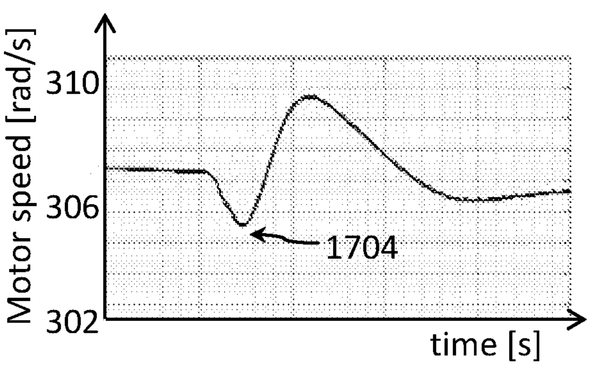



FIG. 17D

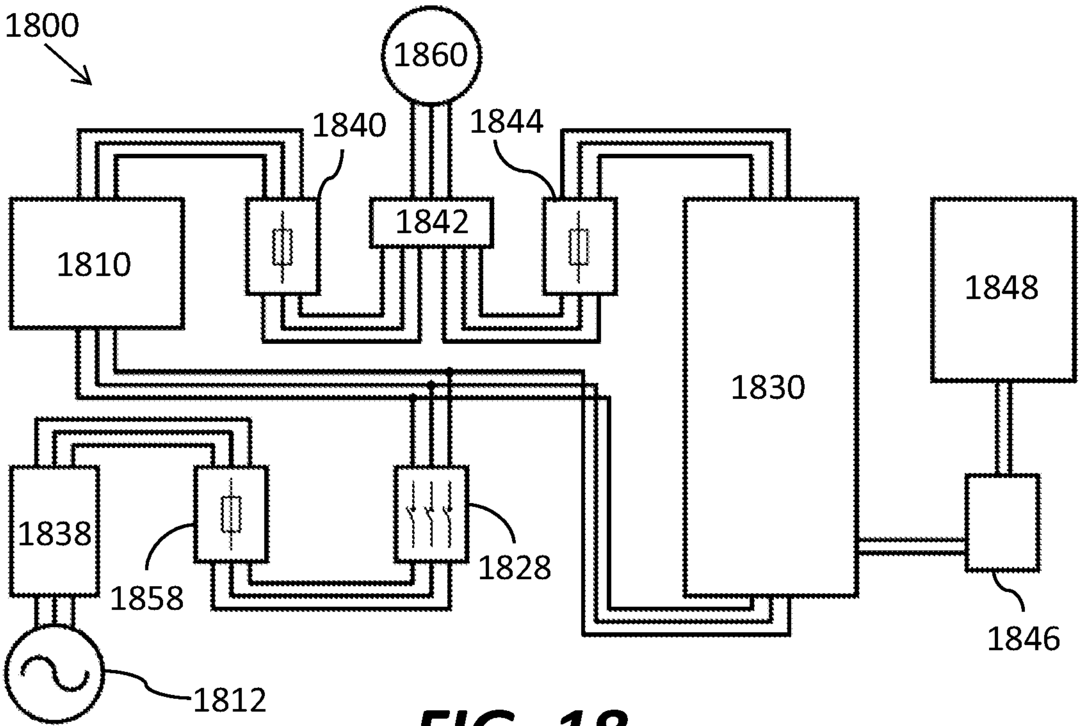



FIG. 18

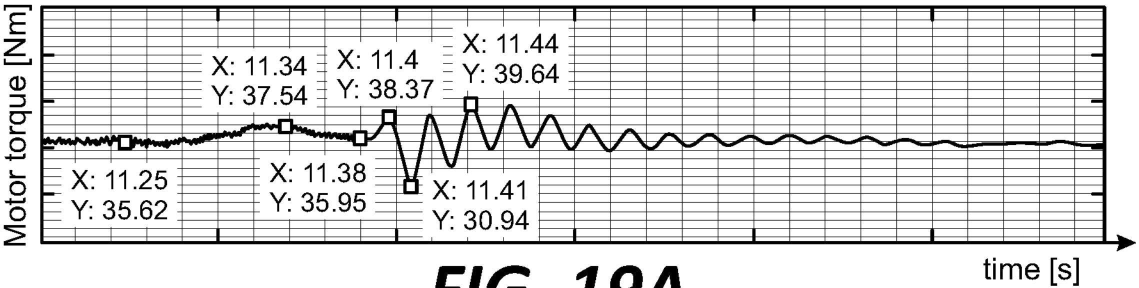



FIG. 19A

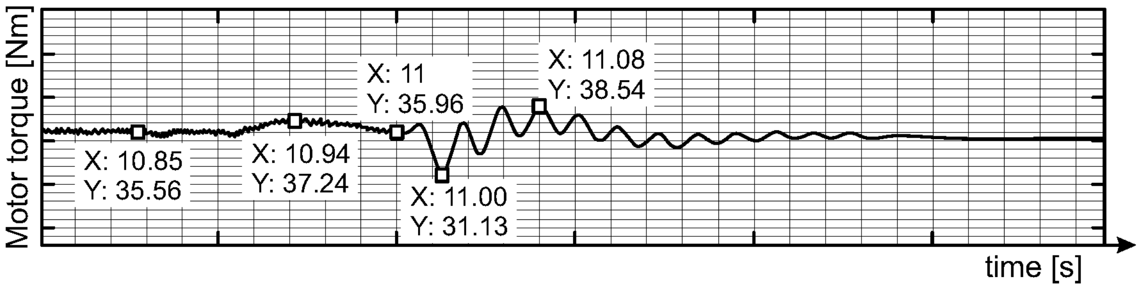



FIG. 19B

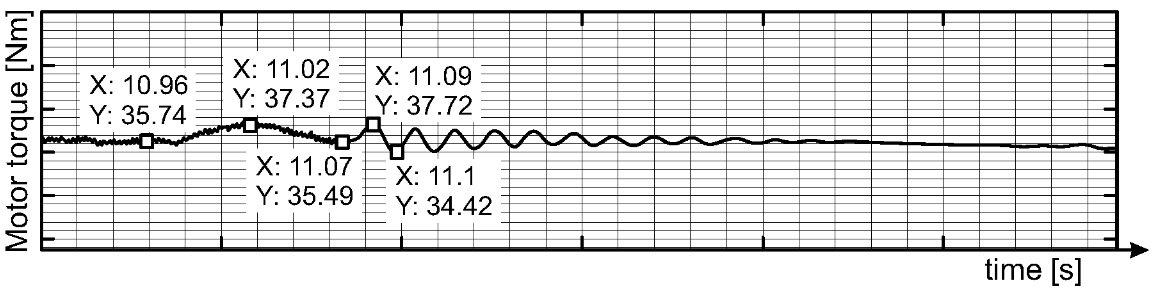



FIG. 19C

# INTERNATIONAL SEARCH REPORT

International application No.
**PCT/IL2025/050174**

**A. CLASSIFICATION OF SUBJECT MATTER**

***H02J 9/06***(2025.01)i; ***H02P 27/04***(2025.01)i
CPC:H02J 9/062; H02J 9/06; H02P 27/04

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H02J 9/06; H02P 27/04
CPC:H02J 9/062; H02J 9/06; H02P 27/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases consulted: Orbit, AI based search

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y | US 2019267836 A1 (ABB Schweiz AG) 29 August 2019 (2019-08-29)<br>entire document | 1-7,17,18<br>8-16,19-27 |
| Y | US 2012187886 A1 (Yaskawa America Inc) 26 July 2012 (2012-07-26)<br>entire document | 8,10-16,20-22 |
| Y | US 2017126164 A1 (Eaton Intelligent Power Ltd) 04 May 2017 (2017-05-04)<br>entire document | 8,10,13,20,21 |
| A | US 2008174257 A1 (Johnson Controls Tyco IP Holdings LLP) 24 July 2008 (2008-07-24)<br>entire document | 1-27 |
| A | US 2018262132 A1 (Regal Beloit America Inc) 13 September 2018 (2018-09-13)<br>entire document | 1-27 |

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
- "D" document cited by the applicant in the international application
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| **27 May 2025** | **27 May 2025** |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**Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel**
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Email: **pctoffice@justice.gov.il**

Authorized officer

**ZAHDEH Jihad**

Telephone No.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | CN 108880402 A (Wolong Electric Group Liaoning Rongxin Electric Transmission Co ltd) 23 November 2018 (2018-11-23)<br>entire document | 1-27 |

**INTERNATIONAL SEARCH REPORT**
**Information on patent family members**

International application No.
**PCT/IL2025/050174**

| Patent document cited in search report | | | Publication date (day/month/year) | Patent family member(s) | | | Publication date (day/month/year) |
|---|---|---|---|---|---|---|---|
| US | 2019267836 | A1 | 29 August 2019 | US | 2019267836 | A1 | 29 August 2019 |
| | | | | US | 11342786 | B2 | 24 May 2022 |
| | | | | CN | 110168852 | A | 23 August 2019 |
| | | | | CN | 110168852 | B | 12 December 2023 |
| | | | | EP | 3539196 | A1 | 18 September 2019 |
| | | | | EP | 3539196 | B1 | 19 May 2021 |
| | | | | ES | 2883718 | T3 | 09 December 2021 |
| | | | | WO | 2018087204 | A1 | 17 May 2018 |
| US | 2012187886 | A1 | 26 July 2012 | US | 2012187886 | A1 | 26 July 2012 |
| | | | | US | 9018882 | B2 | 28 April 2015 |
| US | 2017126164 | A1 | 04 May 2017 | US | 2017126164 | A1 | 04 May 2017 |
| | | | | US | 10033322 | B2 | 24 July 2018 |
| | | | | CA | 3003497 | A1 | 04 May 2017 |
| | | | | CA | 3003497 | C | 07 March 2023 |
| | | | | MX | 2018005214 | A | 15 August 2018 |
| | | | | WO | 2017074508 | A1 | 04 May 2017 |
| US | 2008174257 | A1 | 24 July 2008 | US | 2008174257 | A1 | 24 July 2008 |
| | | | | US | 8014110 | B2 | 06 September 2011 |
| | | | | AT | E478466 | T1 | 15 September 2010 |
| | | | | CN | 101584106 | A | 18 November 2009 |
| | | | | CN | 101584106 | B | 31 October 2012 |
| | | | | CN | 101584262 | A | 18 November 2009 |
| | | | | CN | 101584262 | B | 04 September 2013 |
| | | | | CN | 101589538 | A | 25 November 2009 |
| | | | | CN | 101589538 | B | 20 February 2013 |
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