A Low-Voltage CMOS Multiplier for RF Applications

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ABSTRACT

A low-voltage analog multiplier operating at 1.2V is presented. The multiplier core consists of four MOS transistors operating in the saturation region. The circuit exploits the quadratic relation between current and voltage of the MOS transistor in saturation. The circuit was designed using standard 0.6µm CMOS technology. Simulation results indicate an IP3 of 4.9dBm and a spur free dynamic range of 45dB.

Keywords

Low-voltage, RF, CMOS, analog multiplier.

1. INTRODUCTION

The demand for portable wireless communications systems has motivated the development of low-voltage CMOS RF mixers [1], [5-6]. The design of portable sets follows the trends that include lower cost, longer battery life, smaller size and lower weight. The voltage that is used nowadays is around 3V but very soon lower voltages, close to 1V will be required. Bipolar and GaAs IC's are dominating the RF section of today's wireless transceivers, but CMOS is becoming a viable contender [7]. These mixers have good performances but their use for wireless applications is limited by the relatively high bias voltage required.

Operation at 1V (or a little more) is difficult to achieve with bipolar technology: the V_{BE} is around 0.7V and the base-to-collector junction must be reverse biased. By contrast the MOS transistor can admit a V_{DS} lower than the V_{GS}. Therefore, if the saturation voltage is kept at a few hundred mV there is enough room for some output dynamic range. This paper exploits this key feature.

A low-voltage circuit capable of performing the analog multiplication of two differential input signals, with low-signal distortion and low power dissipation is proposed. The most noticeable feature of the proposed structure is its low-voltage operation. It can operate at a supply voltage of 1.2V while sustaining high linearity making it suitable for battery operated portable systems. The circuit has been designed for a 1.2V, 900MHz application in a 0.6µm standard CMOS process. The principle of operation is described in section 2. In section 3 the circuit realization is given. The simulation results follow in section 4, while a conclusion is given in section 5.

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2. PRINCIPLE OF OPERATION

The block diagram of the proposed multiplier is shown in Fig. 1. The first stage consists of four identical adders producing the sum of their respective input signals together with a dc offset. These outputs are then combined in the second stage to form the multiplication function. The transfer functions of the two blocks forming the multiplier core are given by:

$$Z_i = A_1 v_1^2 + A_2 v_2^2 + A_3 B_i v_1 v_2 + A_4 \quad (i = 1,2) \qquad (1)$$

where Z_i is the output of core i, and $A_1 \sim A_4$ and B_i are constants. The output signal v_{out} is the difference between the outputs Z_1 and Z_2, and results in:

$$v_{out} = A_3(B_1 - B_2)v_1 v_2 = C v_1 v_2 \qquad (2)$$

where C is a constant. Thus the output is a linear multiplication of v_1 and v_2 with multiplication constant C.

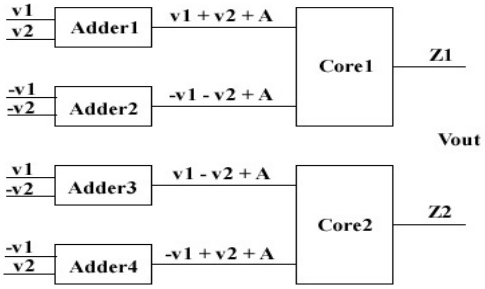

Figure 1. Block Diagram of Multiplier.

3. CIRCUIT REALIZATION

The schematic diagram of the adder circuit is shown in Fig. 2. The transistors M_3 (M_{3a}), M_4 (M_{4a}), and M_5 (M_{5a}) function as a linear resistor giving an output current, I_{o1} (I_{o2}), proportional to the input voltage v_1 (v_2). These currents, I_{o1} and I_{o2}, are added together in the resistor R_{out} providing an output voltage proportional to the sum of the input voltages. Transistors M_1 and M_2 provide a stable biasing for the circuit.

The next stage consists of two identical cores [2]. The schematic diagram of one of these cores is shown in Fig. 3. The circuit exploits the quadratic relation between the current and voltage of the MOS transistor in saturation to produce the required output. The current equation for the MOS transistor in saturation is approximately given by:

$$I_D = K\frac{W}{2L}(V_{GS} - V_{th})^2 \tag{3}$$

where $K = \mu C_{ox}$, W and L are the width and length of the transistor respectively, V_{GS} is the gate to source voltage, and V_{th} is the threshold voltage.

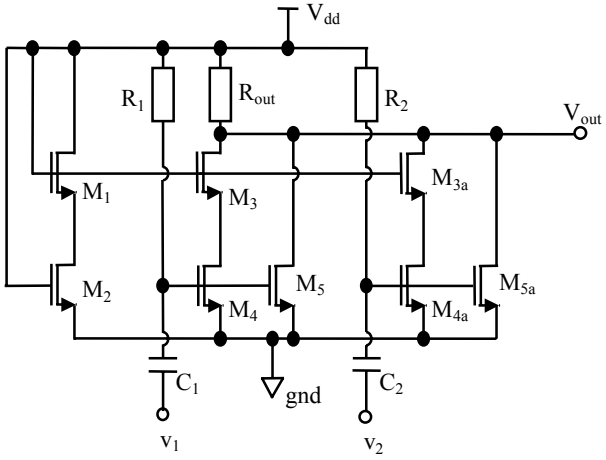

Figure 2. Adder Circuit.

Assuming $V_{GS0} - V_{th} = V_{ov0} = A$, where V_{GS0} and V_{ov0} are the quiescent V_{GS} and quiescent overdrive, respectively, the inputs to the MOS transistors are given by:

$$V_{GS1} - V_{th} = v_1 + v_2 + A \tag{4}$$

$$V_{GS2} - V_{th} = -v_1 - v_2 + A \tag{5}$$

$$V_{GS3} - V_{th} = v_1 - v_2 + A \tag{6}$$

$$V_{GS4} - V_{th} = -v_1 + v_2 + A \tag{7}$$

Thus the current in the MOS transistors is given by:

$$\begin{aligned} I_{D1} &= K'(v_1 + v_2 + A)^2 \\ &= K'\left[v_1^2 + v_2^2 + A^2 + 2v_1v_2 + 2A(v_1 + v_2)\right] \end{aligned} \tag{8}$$

$$\begin{aligned} I_{D2} &= K'(-v_1 - v_2 + A)^2 \\ &= K'\left[v_1^2 + v_2^2 + A^2 + 2v_1v_2 + 2A(-v_1 - v_2)\right] \end{aligned} \tag{9}$$

$$\begin{aligned} I_{D3} &= K'(v_1 - v_2 + A)^2 \\ &= K'\left[v_1^2 + v_2^2 + A^2 - 2v_1v_2 + 2A(v_1 - v_2)\right] \end{aligned} \tag{10}$$

$$\begin{aligned} I_{D4} &= K'(-v_1 + v_2 + A)^2 \\ &= K'\left[v_1^2 + v_2^2 + A^2 - 2v_1v_2 + 2A(-v_1 + v_2)\right] \end{aligned} \tag{11}$$

where K' = KW/2L. These currents are summed up in the respective resistors making up the core, producing the required output voltage. Assuming a perfect match in the components the output voltage is given by:

$$v_{out} = R\left[(I_{D1} + I_{D2}) - (I_{D3} + I_{D4})\right] = 8K'Rv_1v_2 \tag{12}$$

which is the required multiplication.

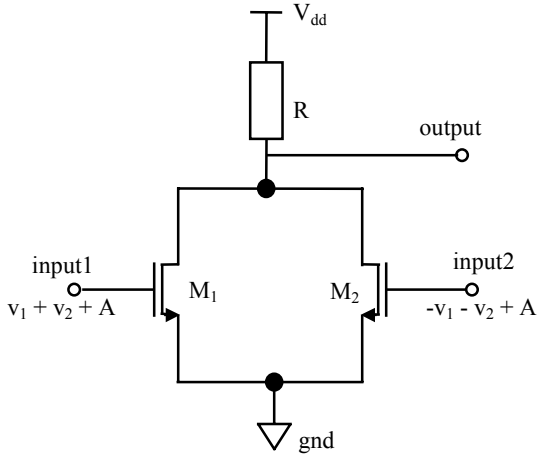

Figure 3. Multiplier Core.

Any variation from the above conditions will produce harmonic components in the output spectrum. Mobility degradation effect and the mismatches in the dimensions of the transistor or resistor values can be accounted for by using a global non-ideality parameter $(1 + \delta)$ in the second term of equation (3). Assuming the non-ideality errors to be uncorrelated and superimposing quadratically their contributions, equation (12) becomes:

$$\begin{aligned} v_{out} &= 8K'Rv_1v_2 \\ &+ 4\delta K'R\left[v_1^2 + v_2^2 + A^2 + 2(v_1v_2 + v_1A + v_2A)\right] \end{aligned} \tag{13}$$

Therefore the output contains only five extra terms, two of these are linear ($8\delta K'Rv_1A$ and $8\delta K'Rv_2A$), two are quadratic ($4\delta K'Rv_1^2$, and $4\delta K'Rv_2^2$) and the other is an offset ($4\delta K'RA^2$). The linear extra terms lie at high frequencies (800MHz and 900MHz in this work), and thus can easily be filtered out using a low-pass filter section after the multiplier. Also the offset term is at dc and can be ignored in most applications. Therefore assuming that the layout of the transistors is carefully designed, we estimate that the δ can be as low as 0.2%. Thus, since the contribution of the extra quadratic terms in equation (13) is equal to δ in the worst condition it can be neglected. From equation (13) the gain of the circuit is given by:

$$v_{out} = 8(1 + \delta)K'Rv_1v_2 \tag{14}$$

This implies that there is also a gain error of $(1 + \delta)$ but since δ is very small it has negligible effect on the circuit's performance.

There is also an additional contribution of the pre-processing adder blocks; however these signals are achieved with suitably high linearity.

4. SIMULATION RESULTS

The circuit has been simulated using a standard 0.6µm double-poly, double-metal CMOS process. The adder circuit has been designed to have a 3dB bandwidth of 1GHz. This ensures that the signals are not attenuated while passing through these adder circuits. The multiplier core was optimized to obtain a high linearity; in order to achieve this goal a compromise had to be found between gain and linearity of the complete circuit. The width-to-length ratios of the multiplier core transistors are 50/0.6. The output currents are converted to a differential voltage through the connection of two 1kΩ resistors.

All the simulations were performed using a 1.2V supply. The differential input sinewaves applied at the input terminals have an amplitude of ±200mV and frequencies of 800MHz and 900MHz at terminals v_1 and v_2 respectively, producing an output at 100MHz.

Fig. 4 shows the simulated dc transfer characteristic of the multiplier with the input voltages v_1 and v_2 varying between -200mV and +200mV, and the corresponding maximum output swing of ±200mV. Fig. 5 illustrates the output spectrum. It shows that the third harmonic component lies 45dB below the fundamental signal. Fig. 6 indicates that the third order intercept point is at 4.9dBm. The circuit was also simulated with a mismatch of 0.2% standard deviation. This leads to additional harmonic terms but the SFDR (Spur Free Dynamic Range) worsens only by about 2dB.

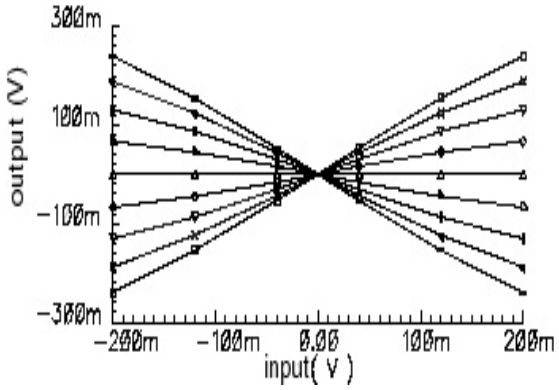

Figure 4. DC Transfer Characteristics.

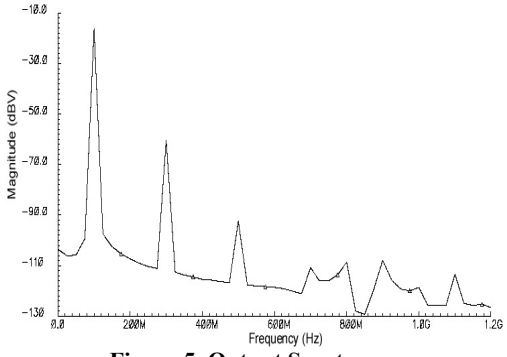

Figure 5. Output Spectrum.

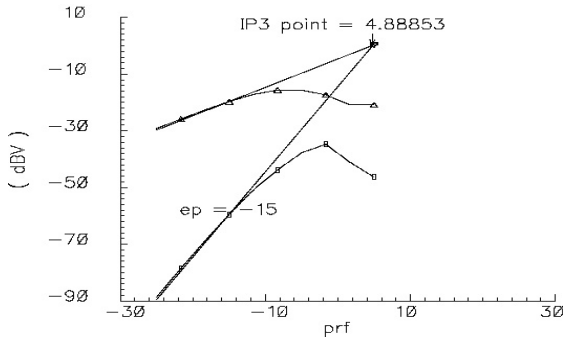

Figure 6. IP3 Point.

5. SUMMARY

A low-voltage CMOS multiplier based on the square law characteristics of MOS devices has been analyzed. The circuit can operate at a 1.2V supply voltage with good simulation results. The results obtained are comparable to a similar architecture proposed recently by Hsiao et al. [3, 4]. The advantages of this circuit in comparison to that proposed by Hsiao et al. [4] is that it is less effected by component mismatch [2]. Simulation results indicate a SFDR of 45dB, and an IP3 of 4.9dBm. The proposed structure is symmetric and occupies a small chip area making it a very feasible analog multiplier in various communication systems.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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