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Compensation techniques for non-linearities in H-bridge inverters

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Abstract

This paper presents compensation techniques for component non-linearities in H-bridge inverters as those used in grid-connected photovoltaic (PV) inverters. Novel compensation techniques depending on the switching device current were formulated to compensate for the non-linearities in inverter circuits caused by the voltage drops on the switching devices. Both simulation and experimental results will be presented. Testing was carried out on a PV inverter which was designed and constructed for this research. Very satisfactory results were obtained from all the compensation techniques presented, however the exact compensation method was the most effective, providing the highest reduction in harmonics.

Keywords: Inverters; Dead time; Non-linearities; Switching devices; Voltage drop; Photovoltaic

1. Introduction

Grid-connected PV inverter systems have become an attractive renewable energy generating method and the number of these systems connected to the grid is always increasing. Therefore it is of high importance that the harmonics generated by these inverters are limited to minimize adverse effects on the grid power quality. This means that the design of these inverters should follow harmonic limits set by IEEE and European IEC standards which suggest limits for the current total harmonic distortion (THD) factor and also for the magnitude of each harmonic (IEEE, 2000; IEEE, 2003; IEC, 2004).

The quality of the voltage and current provided by grid-connected inverters is affected by a number of factors. The current controller of the inverter like the Proportional-Integral (PI) or the Proportional-Resonant (PR) controller can have a significant effect on the quality of the current supplied to the grid by the PV inverter, and therefore it is important that the controller provides a high quality sinusoidal output with minimal distortion to avoid creating harmonics as discussed in Zammit et al. (2014a,b). Another factor affecting the quality of the inverter output current

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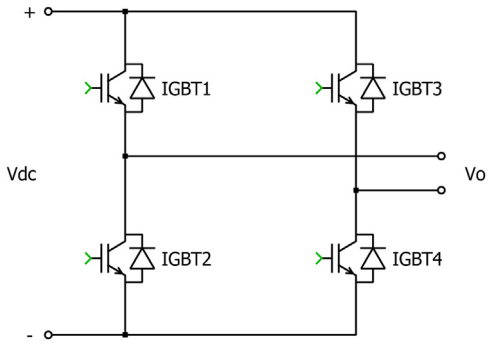


Fig. 1. Single phase IGBT inverter.

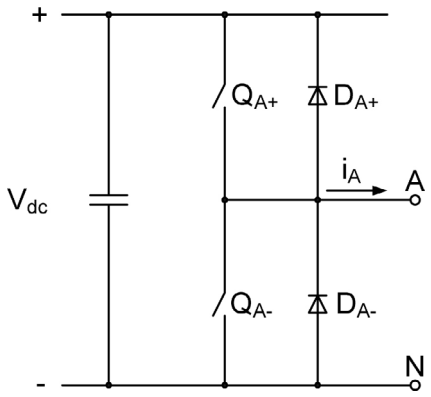


Fig. 2. One leg of a single phase or three phase inverter.

when it is grid-connected is the harmonics already present in the grid supply, which are due to other non-linear loads connected to the grid. Another two factors which affect the amount of harmonics in the inverter output current and voltage resulting from the non-ideal nature of a H-bridge inverter are the distortion due to the inverter dead time, and the distortion caused by the component non-linearities, mainly the voltage drops on the switching components of the inverter itself.

One method to compensate for harmonics in grid connected inverters is by using additional PR harmonic compensators on individual harmonics which need to be reduced (Zammit et al., 2014b; Teodorescu et al., 2004; Liserre et al., 2005; Ciobotaru et al., 2005; Teodorescu et al., 2006; Castilla et al., 2009; Zmood and Holmes, 2003; Teodorescu et al., 2011). Other methods presented in Zhang and Xu (2014) and Li et al. (2015) deal with the reduction and compensation of the harmonics caused by the distortion created by the dead time. However, limited literature was found about methods to specifically compensate the harmonics in the inverter output current and voltage caused by the distortion created by the component non-linearities like the voltage drops on the switching components. This type of compensation will be dealt with in this paper, in addition to dead time compensation, by considering a single phase H-bridge inverter as shown in Fig. 1.

2. Non-linearities

2.1. Dead time/blanking time

If the switching devices of one leg of the inverter shown in Fig. 2 are assumed to be ideal, the states of the two switching devices (Q_{A+} and Q_{A-}) can be changed simultaneously from on to off and vice versa. In practice switching devices have finite turn-on and turn-off delays and there can also be differences in timing delays between the gate circuitry driving switches Q_{A+} and Q_{A-}. Therefore the turn-on of the switching devices is delayed by a few

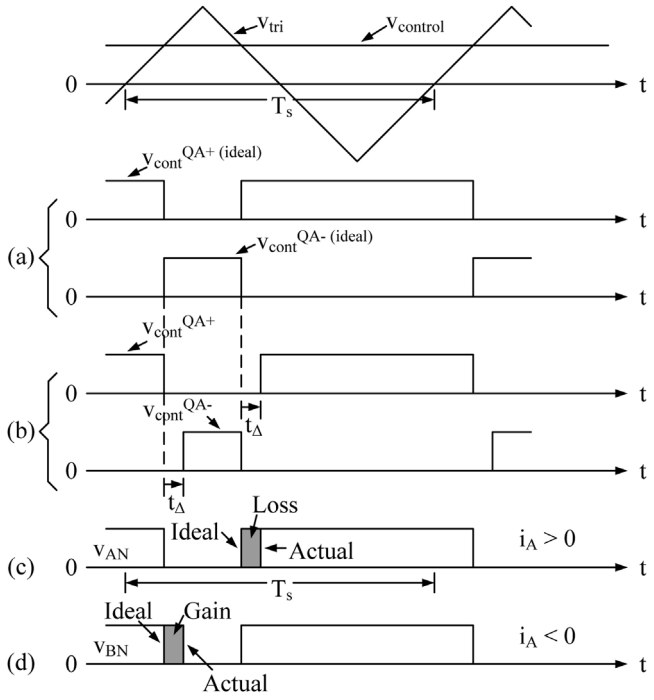


Fig. 3. Effect of dead time/blanking time.

microseconds to prevent the probability of having both switches in a leg turned on at the same time for the transition period.

The switching instant is determined by the comparison of the triangular waveform (v_{tri}) and the control voltage ($v_{control}$), and in ideal switching devices (Q_{A+} and Q_{A-}) the change over from on to off and vice versa happens simultaneously as shown in Fig. 3(a). In practice a switching device is turned off at the instant determined by the comparison of the triangular waveform (v_{tri}) and the control voltage ($v_{control}$) but the turn-on of the other switch is delayed by a few microseconds as shown in Fig. 3(b). This time is called Dead Time or Blanking Time (t_Δ) where both upper and lower switches are off, and this avoids 'shoot through' or cross-conduction current through the leg. The slower the switching device, the larger is the dead time needed. The dead time introduces a non-linearity which causes distortion in the output voltage and current, and therefore the smaller is the dead time the better.

The implementation of PWM inside a microcontroller is carried out using a counter instead of the triangular waveform to determine the on and off instants. However to understand better the effect of dead time, it is more convenient to use the waveforms shown in Fig. 3.

Since both switches of the leg are off during the dead time the output voltage of the leg v_{AN} depends on the direction of the current i_A as shown in Fig. 3(c) for $i_A > 0$ and in Fig. 3(d) for $i_A < 0$ (Mohan et al., 2003). The ideal waveforms without dead time are shown for both cases in Fig. 3(c) and (d). There is a decrease in the pulse width when the current is greater than zero ($i_A > 0$) as shown in Fig. 3(c) and there is an increase in the pulse width when the current is less than zero ($i_A < 0$) as shown in Fig. 3(d).

The difference in the leg output voltage is given by:

$$v_e = v_{an(ideal)} - v_{AN(actual)} \tag{1}$$

By taking the average of v_e over one switching period, we can obtain the change (defined as a drop if positive) in the leg output voltage due to the dead time (t_Δ) for leg A:

$$\begin{aligned} \Delta V_{AN} &= +\frac{t_\Delta}{T_s} V_{dc} \quad \text{if} \quad i_A > 0 \\ \Delta V_{AN} &= -\frac{t_\Delta}{T_s} V_{dc} \quad \text{if} \quad i_A < 0 \end{aligned} \tag{2}$$

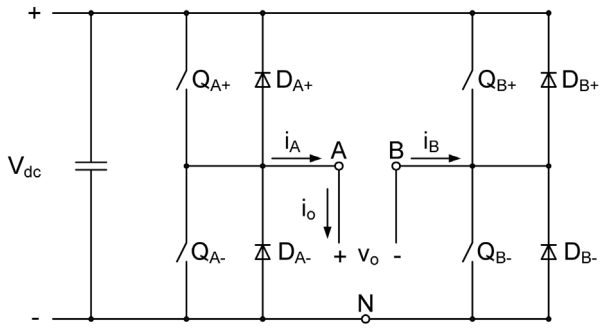


Fig. 4. Single phase inverter with current flow.

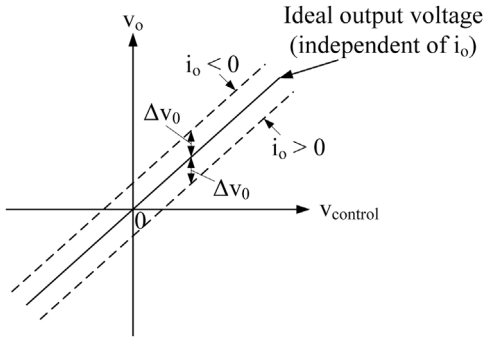


Fig. 5. Plot of V_o as a function of $v_{control}$.

From Eq. (2) it can be observed that the polarity of the change in the leg output voltage ΔV_{AN} depends on the current direction. ΔV_{AN} is proportional to the dead time t_Δ and the switching frequency f_s (=$1/T_s$), therefore at higher switching frequencies, faster switching devices that allow t_Δ to be small should be used (Mohan et al., 2003).

By applying the same analysis to leg B shown in Fig. 4, and since $i_A = -i_B$:

$$\begin{aligned} \Delta V_{BN} &= -\frac{t_\Delta}{T_s} V_{dc} \quad \text{if} \quad i_A > 0 \\ \Delta V_{BN} &= +\frac{t_\Delta}{T_s} V_{dc} \quad \text{if} \quad i_A < 0 \end{aligned} \tag{3}$$

$$\text{Since,} \quad \text{the output voltage} \quad v_o = v_{AN} - v_{BN} \tag{4}$$

$$\text{and,} \quad \text{output current} \quad i_o = i_A \tag{5}$$

the instantaneous average output voltage developed over a switching period differs from the desired value by ΔV_o, given by:

$$\begin{aligned} \Delta V_o = \Delta V_{AN} - \Delta V_{BN} &= +\frac{2t_\Delta}{T_s} V_{dc} \quad \text{if} \quad i_o > 0 \\ \Delta V_o = \Delta V_{AN} - \Delta V_{BN} &= -\frac{2t_\Delta}{T_s} V_{dc} \quad \text{if} \quad i_o < 0 \end{aligned} \tag{6}$$

Fig. 5 shows a plot of the instantaneous average output voltage V_o as a function of $v_{control}$ showing the effect of the dead time t_Δ, where ΔV_o is defined as a voltage drop when it is positive. Fig. 6 shows the distortion effect of the dead time t_Δ on the sinusoidal waveform of the instantaneous average output voltage $v_o(t)$, for a sinusoidal $v_{control}$ and for a load current i_o which is assumed to be sinusoidal and lagging behind $v_o(t)$, in a single phase full bridge PWM inverter.

The distortion in $v_o(t)$ at the current zero crossings causes low order harmonics such as third, fifth, seventh and so on, of the fundamental frequency in the inverter output (Mohan et al., 2003).

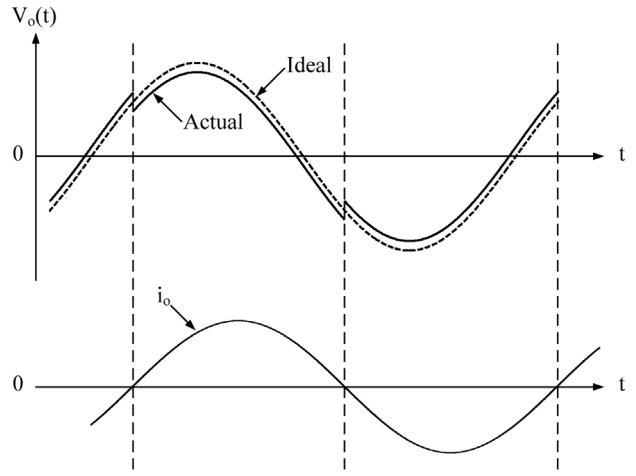


Fig. 6. Effect of t_Δ on the sinusoidal waveform of the instantaneous average output voltage.

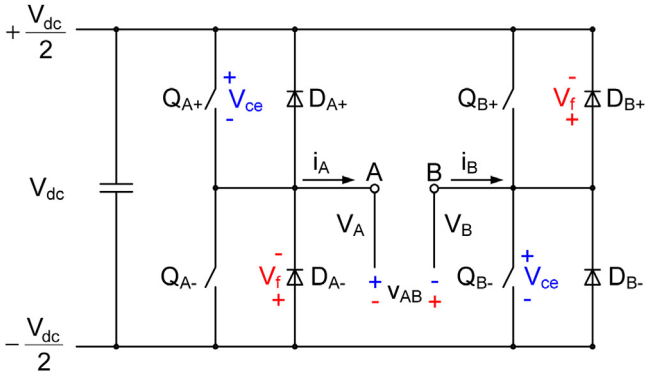


Fig. 7. +ve current flow.

2.2. Switching device voltage drops

Another non-linearity in the output inverter voltage and current is caused by the device voltage drops on the switching devices, in this case the IGBTs and the Freewheeling Diodes. The device voltage drops can be divided into two; the on-state zero current device drops and the device drops due to the on-state resistance R_{on}. These device drops can be defined by the procedure that follows.

Fig. 7 shows the current flow when the current is positive, i.e. flowing from A to B. When Q_{A+} and Q_{B-} are gated on, current flows through the devices and the corresponding component voltage drops and the voltage polarity of V_{AB} are shown in blue. When Q_{A+} and Q_{B-} are off and current is positive, D_{A-} and D_{B+} conduct and the corresponding component voltage drops and the voltage polarity of V_{AB} are shown in red.

When the current i_A is positive, for a switching period T_s, and taking the duty cycle for leg A to be d_A, the voltage at A (V_A) can be described by:

$$v_{A\_ideal} = d_A \frac{V_{dc}}{2} + (1 - d_A)\left(-\frac{V_{dc}}{2}\right) = (2d_A - 1)\left(\frac{V_{dc}}{2}\right) \tag{7}$$

where V_{dc} is the dc-link voltage, and

$$v_{A\_actual} = d_A\left(\frac{V_{dc}}{2} - V_{IGBT}\right) + (1 - d_A)\left(-\frac{V_{dc}}{2} - V_{Diode}\right) = (2d_A - 1)\left(\frac{V_{dc}}{2}\right) - d_A V_{IGBT} - (1 - d_A) V_{Diode} \tag{8}$$

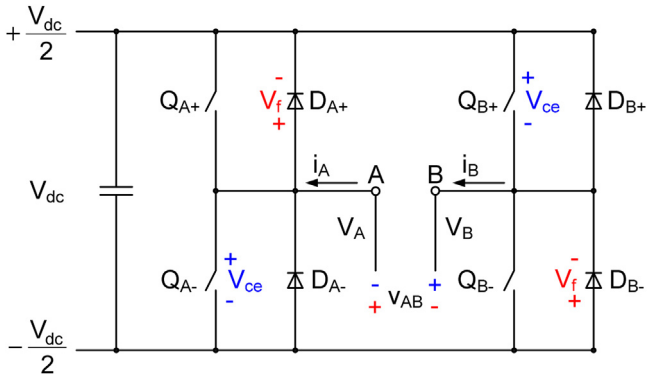


Fig. 8. −ve current flow.

where V_{IGBT} is the voltage drop on the IGBT, and V_{Diode} is the forward voltage drop on the diode.

Therefore, the error in V_A is:

$$v_{A\_error} = -d_A V_{IGBT} - (1 - d_A)V_{Diode} \quad \text{when} \quad i_A > 0 \tag{9}$$

When the current i_B is positive, for a switching period T_s, and taking the duty cycle for leg B to be d_B, the voltage at B (V_B) can be described by:

$$v_{B\_ideal} = d_B \frac{V_{dc}}{2} + (1 - d_B)\left(-\frac{V_{dc}}{2}\right) = (2d_B - 1)\left(\frac{V_{dc}}{2}\right) \tag{10}$$

and

$$v_{B\_actual} = d_B\left(\frac{V_{dc}}{2} + V_{Diode}\right) + (1 - d_B)\left(-\frac{V_{dc}}{2} + V_{IGBT}\right) = (2d_B - 1)\left(\frac{V_{dc}}{2}\right) + d_B V_{Diode} + (1 - d_B)\, V_{IGBT} \tag{11}$$

Therefore, the error in V_B is:

$$V_{B\_error} = d_B V_{Diode} + (1 - d_B)V_{IGBT} \quad \text{when} \quad i_B > 0 \tag{12}$$

Fig. 8 shows the current flow when the current is negative, i.e. flowing from B to A. When Q_{B+} and Q_{A-} are gated on, current flows through the devices and the corresponding component voltage drops and the voltage polarity of V_{AB} are shown in blue. When Q_{B+} and Q_{A-} are off and current is negative, D_{B-} and D_{A+} conduct and the corresponding component voltage drops and the voltage polarity of V_{AB} are shown in red.

Following a similar procedure as the one used to obtain the error in V_A and V_B for a positive current flow, the errors in V_A and V_B for a negative current flow can be obtained.

When the currents i_A and i_B are negative the error in V_A and V_B are:

$$v_{A\_error} = d_A V_{Diode} + (1 - d_A)V_{IGBT} \quad \text{when} \quad i_A < 0 \tag{13}$$

$$v_{B\_error} = -d_B V_{IGBT} - (1 - d_B)V_{Diode} \quad \text{when} \quad i_B < 0 \tag{14}$$

To summarize the errors:

$$\begin{aligned} v_{A\_error} &= -d_A V_{IGBT} - (1 - d_A)V_{Diode} \quad \text{when} \quad i_A > 0 \\ v_{A\_error} &= d_A V_{IGBT} + (1 - d_A)V_{IGBT} \quad \text{when} \quad i_A < 0 \end{aligned} \tag{15}$$

$$\begin{aligned} v_{B\_error} &= d_B V_{Diode} + (1 - d_B)V_{IGBT} \quad \text{when} \quad i_B > 0 \\ v_{B\_error} &= -d_B V_{IGBT} - (1 - d_B)V_{Diode} \quad \text{when} \quad i_B < 0 \end{aligned} \tag{16}$$

3. Compensation

3.1. Dead time/blanking time compensation

As discussed earlier the dead time creates an error represented by (6) in the output voltage. Therefore, (6) can be used to compensate this error by compensating the output voltage.

In this research the dead time t_Δ for the inverter was set to be 0.5 μs and the switching period T_s was set to be 100 μs. Therefore, the voltage difference compensation is given by:

$$\begin{aligned} &\Delta V_o = +\frac{2}{200}V_{dc} \quad \text{when output current} \quad i_o > 0 \\ &\text{and} \\ &\Delta V_o = -\frac{2}{200}V_{dc} \quad \text{when output current} \quad i_o < 0 \end{aligned} \tag{17}$$

This means that for a single leg the dead time compensation voltage V_{dtc} is given by:

$$\begin{aligned} &V_{dtc} = +\frac{V_{dc}}{200} \quad \text{if} \quad i_o > 0 \\ &\text{and} \\ &V_{dtc} = -\frac{V_{dc}}{200} \quad \text{if} \quad i_o < 0 \end{aligned} \tag{18}$$

3.2. Switching device voltage drops compensation

From (15) and (16), the voltage drop compensation equations can be obtained, given by:

$$\begin{aligned} v_{A\_comp} &= d_A V_{IGBT} + (1 - d_A)V_{Diode} \quad \text{when} \quad i_A > 0 \\ v_{A\_comp} &= -d_A V_{Diode} - (1 - d_A)V_{IGBT} \quad \text{when} \quad i_A < 0 \end{aligned} \tag{19}$$

$$\begin{aligned} v_{B\_comp} &= -d_B V_{Diode} - (1 - d_B)V_{IGBT} \quad \text{when} \quad i_B > 0 \\ v_{B\_comp} &= d_B V_{IGBT} + (1 - d_B)V_{Diode} \quad \text{when} \quad i_B < 0 \end{aligned} \tag{20}$$

This compensation has to be added to the control voltage value which controls the PWM output.

In order to apply compensation the IGBTs and diodes forward characteristics have to be known. The characteristics were modeled using piece-wise linear models of the following:

$$V_{IGBT} = V_{ce0} + I_c r_{ce} \tag{21}$$

$$V_{Diode} = V_{f0} + I_d r_d \tag{22}$$

where V_{ce0} is the zero current on-state collector-emitter voltage, r_{ce} is the on-state collector-emitter resistance, V_{f0} is the zero current diode forward voltage, r_d is the on-state forward diode resistance, I_c is the collector current and I_d is the diode current.

The 3 kW inverter used for this research was designed and built using the Semitop 3 SK30GH123 IGBT H-Bridge module. The IGBT and diode characteristics for this module, obtained from the datasheet, were V_{ce0} of 1.5 V, r_{ce} of 67.5 mΩ, V_{f0} of 1 V and r_d of 37.5 mΩ. For more accurate results, characterization tests were carried out on the IGBT H-Bridge module used, obtaining the values; $V_{ce0} = 1.15$ V, $r_{ce} = 112.05$ mΩ, $V_{f0} = 1.15$ V and $r_d = 70.49$ mΩ.

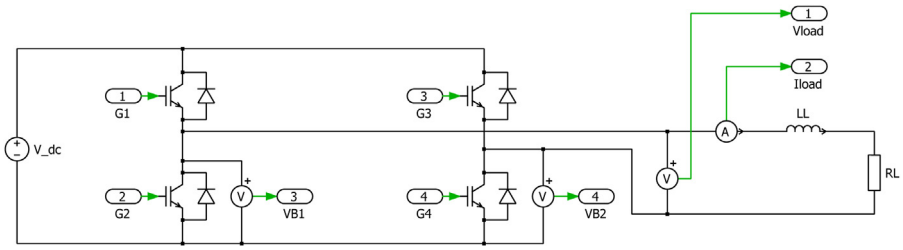


Fig. 9. Inverter model in plecs with resistive and inductive load.

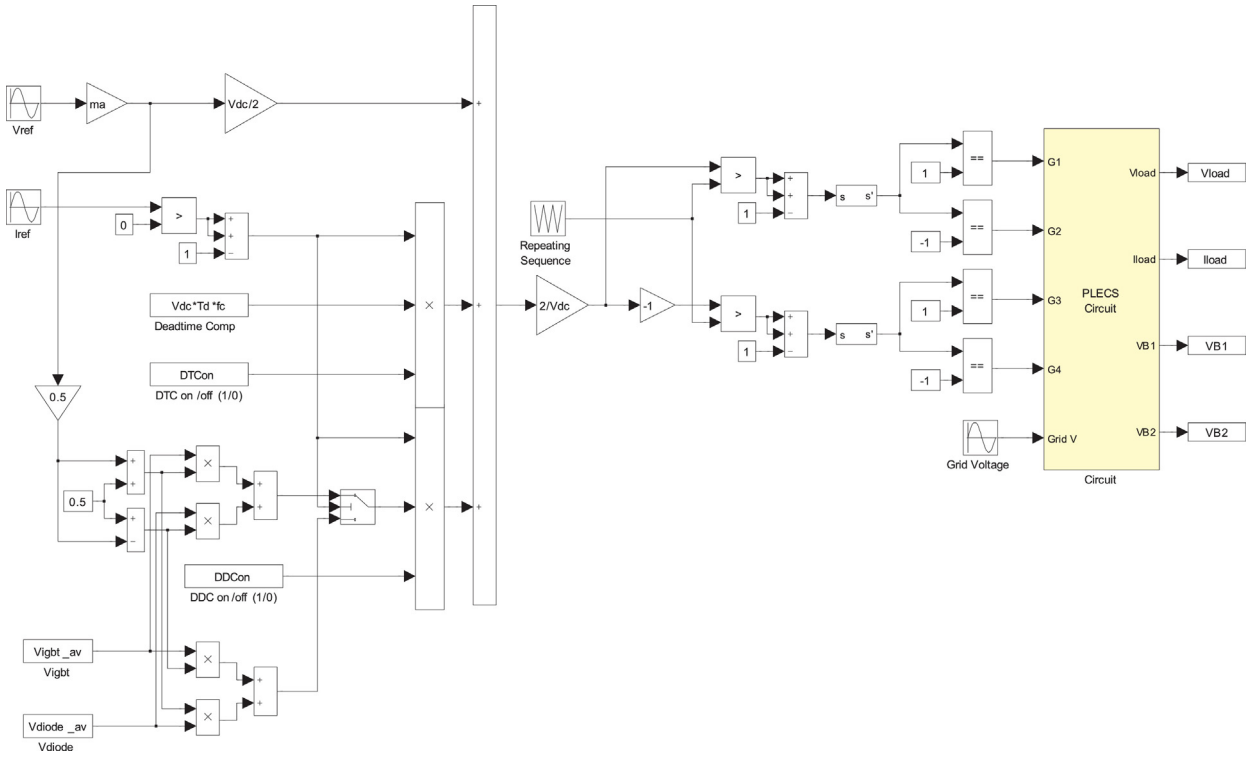


Fig. 10. Dead time and voltage drop compensation simulation model.

4. Dead time and device drop compensation simulations

Simulations with the dead time and device drop compensation were performed using two different methods:

- Voltage compensation by calculating the compensation voltage value using the average inverter current.
- Voltage compensation by calculating the exact value of compensation voltage needed using the instantaneous inverter current.

The simulations were performed with the inverter connected to a resistive load R_L of 0.5 Ω, together with an inductor L_L of 1.2 mH which should draw a load current of about 11.29 A rms. The inverter parameters used for the simulations were; DC-link voltage V_{dc} of 120 V, reference voltage V_{ref} of 10 V peak, switching frequency f_s of 10 kHz and dead time T_d of 0.5 μs. The inverter modeled in Plecs is shown in Fig. 9. The characteristics considered in the models for the IGBTs and diodes were $V_{ce0} = 1.15$ V, $r_{ce} = 112.05$ mΩ, $V_{f0} = 1.15$ V and $r_d = 70.49$ mΩ. In these simulations the inverter was operated in open loop. Fig. 10 shows the inverter with the compensation modeled in Simulink and Plecs,

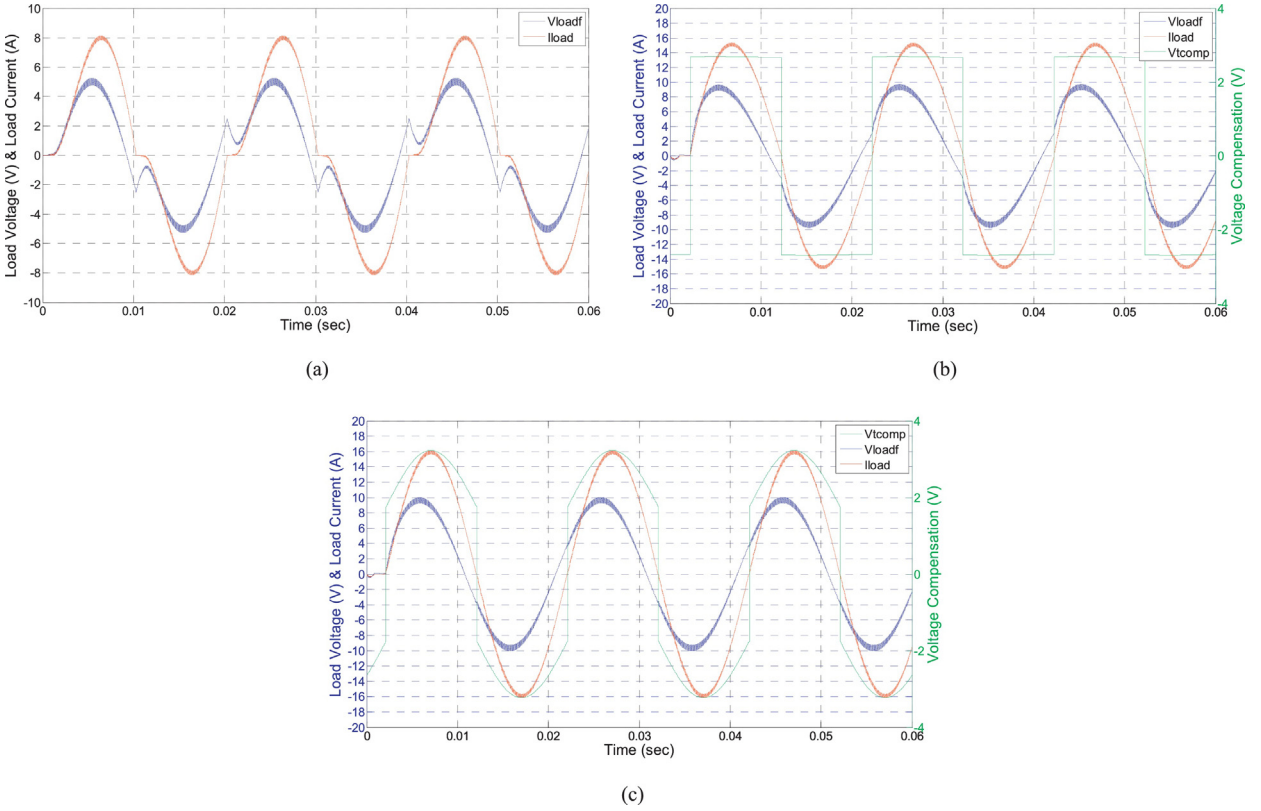


Fig. 11. Load voltage (V_{loadf}) and load current (I_{load}) (a) without compensation, (b) with the compensation voltage (V_{tcomp}) calculated using the average load current, (c) with the compensation voltage (V_{tcomp}) calculated using the instantaneous load current ($R_L = 0.5\,\Omega$ and $L_L = 1.2\,\text{mH}$).

including both the dead time and the device drop compensations. This model obtains the compensation voltage by using the average inverter current.

Fig. 11(a) shows the filtered load voltage V_{loadf} and the load current I_{load} without compensation. As can be clearly observed the resulting load voltage and load current are far from being sinusoidal which indicates a high amount of harmonics, caused by the inverter non-linearities. Fig. 11(b) and (c) shows the filtered load voltage V_{loadf}, the load current I_{load} and the compensation voltage V_{tcomp} which includes both the dead time and the device drop compensations. In the result of Fig. 11(b) the simulation was performed with the compensation calculated using the average load current and not the instantaneous current, which leads to a small inaccuracy in the compensation, resulting in waveforms where distortion is still present but reduced. In the result of Fig. 11(c) the simulation was performed with the compensation calculated using the instantaneous load current. As can be noted, the load voltage and load current are practically sinusoidal, which clearly demonstrates the effectiveness of the compensation technique.

5. Experimental results with the dead time and device drop compensation

Practical tests with the inverter were carried out to test the compensation techniques. Figs. 12 and 13 show a block diagram of the test setup with the inverter connected to a load and the inverter test rig, respectively. The inverter was operated under open loop control with a resistive load R_L of $0.5\,\Omega$ and an inductor L_i of 1.2 mH. The inverter was controlled by the dsPIC30F4011 microcontroller from Microchip. Through the use of the microcontroller a sinusoidal voltage of 10 V peak was requested at the inverter output. Tests were performed with a low fundamental voltage leading to increased evidence of any harmonic distortion in the resultant waveforms. The dc-link voltage V_{dc} was set to 120 V. An analysis on the test results was carried out to analyze the inverter output voltage and current with and without the dead time and device drop compensation, in each case observing the harmonic spectrum.

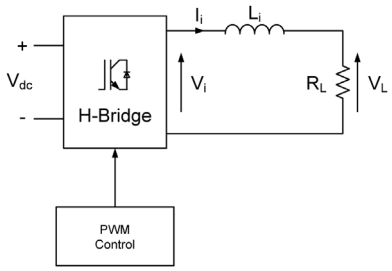


Fig. 12. Compensation testing setup with the inverter connected to a load.

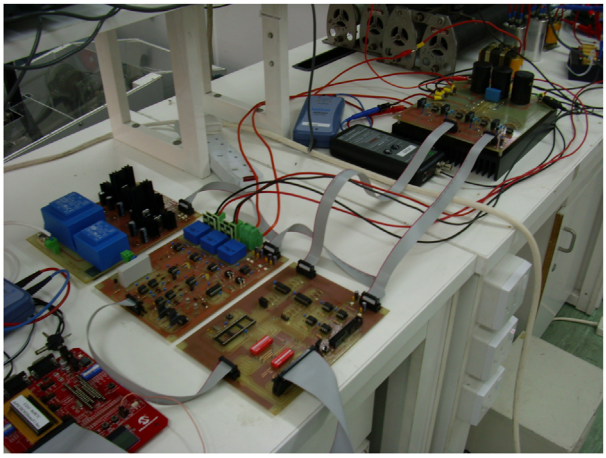


Fig. 13. Inverter test rig.

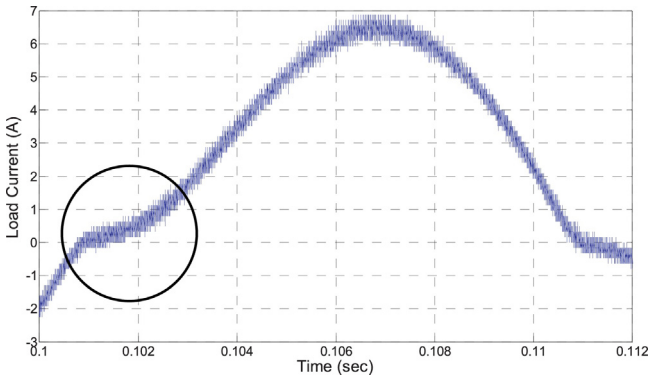


Fig. 14. Load current around the zero-crossing.

5.1. Obtaining the compensation timing

A very important factor in applying the compensation is that it is applied at the correct time. Incorrect application of the compensation leads to a more distorted voltage and current waveforms, thus resulting in more harmonic content. The compensation should be correctly applied according to the direction of the current. Therefore, accurate sensing of the current direction is required. This becomes problematic if the current being sensed is distorted, especially if it exhibits crossover distortion as shown in Fig. 14.

In order to illustrate the full potential of the compensation technique when implementation is not constrained by software delays, an open loop compensation technique was applied with a predetermined sinusoidal load current waveform with current magnitude and phase delay set according to the load used and the fundamental voltage applied.

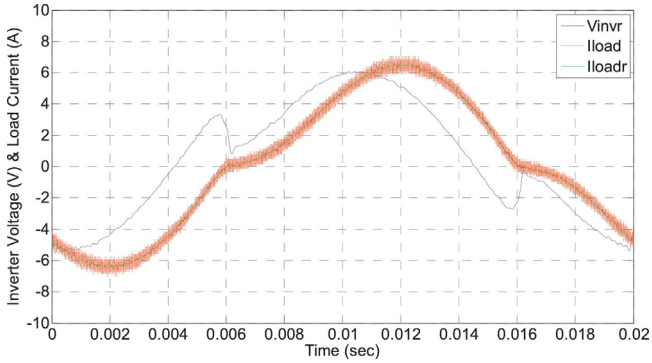


Fig. 15. V_{invr}, I_{load} and I_{loadr} from the inverter connected to a 0.5 Ω load without compensation.

In order to improve compensation accuracy the compensation technique was calibrated through tests carried out with the inverter connected to the load as stated earlier. The timing was obtained by observing the phase shift between the output voltage and the output load current, and observing also the moment any applied compensation takes place, by analyzing the data obtained from the oscilloscope. The data for the inverter voltage and the load current were plotted in Matlab as can be seen in Fig. 15.

The inverter waveforms shown in Fig. 15 represent the low order harmonic content of the inverter output waveforms. The inverter output voltage and current were sampled at high frequency and an FFT was performed in Matlab on the sampled data. The waveforms shown are the reconstruction of the first 13 harmonics from the FFT results for the inverter voltage (V_{invr}) and load current (I_{loadr}). The sampled load current (I_{load}) is also shown. The requested voltage in the test was 10 V peak with the inverter connected to a 0.5 Ω load without compensation. One can note the drop in the voltage waveform when the load current crosses zero, after which the voltage will start to gain its magnitude slowly but never reaches the requested voltage output.

Fig. 16(a) shows the inverter voltage V_{invr} and the fundamental component of the inverter voltage $V_{invfund}$ when compensation is applied with a delay. When the current crosses zero the inverter voltage experiences a drop in the magnitude, and then recovers fast when compensation kicks in. Fig. 16(b) shows the inverter voltage V_{invr} and the fundamental component of the inverter voltage $V_{invfund}$ when the compensation timing is applied correctly.

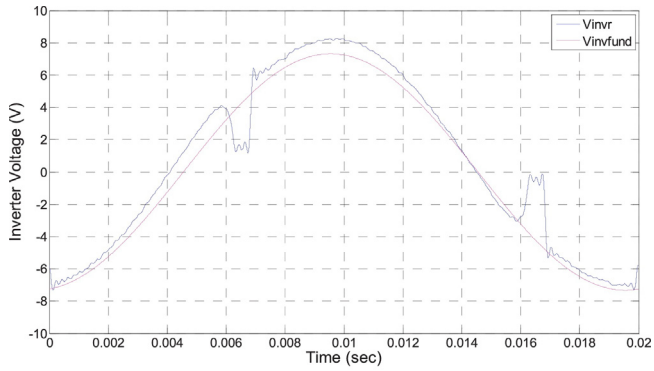
Therefore, the procedure that was used to apply the compensation voltage correctly is to, calculate the phase difference between the inverter voltage and current according the load, and apply this phase shift to the current reference. Fine tuning of the shift can then be performed by observing the moment the compensation voltage is really being applied, by analyzing the inverter voltage waveform as shown in Fig. 16(a) and (b).

5.2. Testing with a 0.5 Ω resistive load

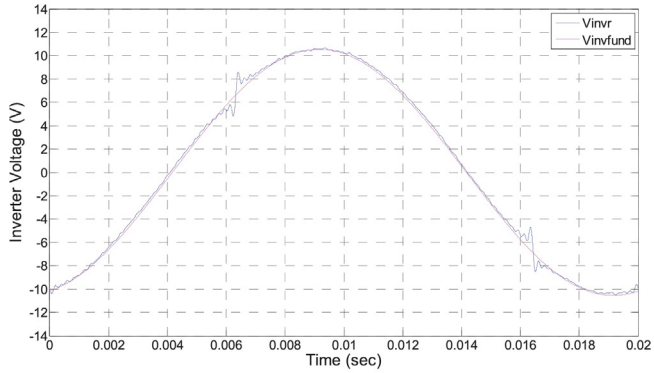
The inverter was connected to a 0.5 Ω wire-wound resistive load and a 1.2 mH inductor. With this load and an inverter output voltage of 10 V peak at a frequency of 50 Hz, the load current was expected to be 15.97 A peak. However from measurements taken, the total inductance measured at the output of the inverter was of 1.33 mH. Therefore the load current expected was of 15.3 A peak. The load current value of 15.3 A peak was used as the base current in the analysis of the results. From the tests performed to obtain the compensation timing, the compensation timing was found to correspond to a phase shift of 36.25°, which should be converted to the corresponding timing to be applied into a microcontroller. This compensation timing was used to obtain the current reference for this particular load.

To obtain a plot of the device drop compensation (without dead time compensation) the device drops for the IGBTs and diodes were modeled as piece-wise current dependent models and calculated using Matlab. Fig. 17 shows the voltage errors for the two legs of the inverter (V_{error1} and V_{error2}), with a load current of 15.3 A peak. Fig. 18 shows the output voltage error, and therefore the output voltage compensation required for a load current of 15.3 A peak.

Testing with the device drop compensation, in addition to the dead time compensation, was performed using three different methods:



(a)



(b)

Fig. 16. Inverter voltage (a) with delay in the compensation, (b) with correctly timed compensation.

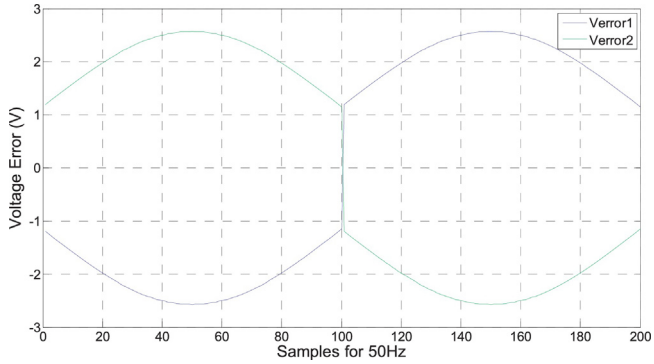


Fig. 17. Voltage error for the inverter legs with a current of 15.3 A peak.

- Voltage compensation using a constant compensation value which reflects the average compensation needed, obtained by averaging the output voltage error calculated using Matlab. The average voltage compensation applied was 4.104 V.
- Voltage compensation by calculating the compensation value using the average inverter current (average current value: $(2 \times I_{load}$ peak)/π A).
- Voltage compensation by calculating the exact value of compensation voltage needed using the instantaneous inverter current.

Fig. 19 shows the inverter voltage and the corresponding voltage harmonic spectrum; (a) without compensation voltage, (b) with average voltage compensation, (c) with the voltage compensation calculated using the average

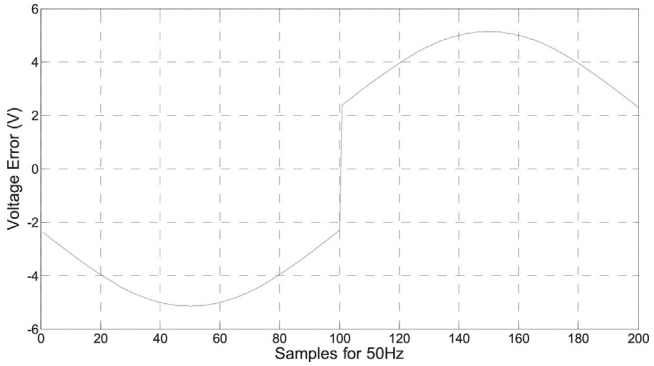


Fig. 18. Output voltage error for the inverter with a current of 15.3 A peak.

Table 1
Harmonics for the inverter connected to a load.

Inverter connected to a 0.5 Ω resistive load								
	Fundamental		3th Harmonic		5th Harmonic		7th Harmonic	
	V_{inv}	I_{load}	V_{inv}	I_{load}	V_{inv}	I_{load}	V_{inv}	I_{load}
Without compensation	50%	47.459%	11.773%	6.331%	6.195%	2.053%	3.847%	0.87%
Average compensation	100%	96.075%	7.696%	3.378%	4.974%	1.226%	4.198%	0.746%
Compensation using I mean	100%	95.888%	7.156%	3.336%	5.16%	1.333%	4.131%	0.778%
Exact compensation	100%	99.108%	0.474%	0.951%	0.68%	0.303%	0.73%	0.313%

load current, and (d) with the exact voltage compensation calculated using the instantaneous current. $V_{invfund}$ and V_{invr} are the fundamental component and the reconstruction up to the 13th harmonic of the inverter voltage analyzed using Matlab, respectively. Fig. 20 shows the load current for a resistive load of 0.5 Ω and the corresponding current harmonic spectrum; (a) without compensation voltage, (b) with average voltage compensation, (c) with the voltage compensation calculated using the average load current, and (d) with the exact voltage compensation calculated using the instantaneous current. I_{load} is the load current, whereas $I_{loadfund}$ and I_{loadr} are the fundamental component and the reconstruction up to the 13th harmonic of the load current analyzed using Matlab, respectively.

6. Comparison of results

Table 1 shows the percentage fundamental and harmonics for the inverter voltage V_{inv} and in the load current I_{load}, worked on the base of the requested inverter output voltage of 10 V peak and the expected load current of 15.3 A peak, as stated earlier. As can be observed from Table 1 all the voltage compensation methods decreased the harmonics in the inverter voltage V_{inv} and in the load current I_{load}. As expected, the compensation voltage applied by the exact compensation method was the most effective in decreasing the harmonics in both the voltage and current. The 3rd, 5th and 7th harmonics in the inverter voltage were reduced by 95.97%, 89.02% and 81.02%, respectively. The 3rd, 5th and 7th harmonics in the load current were reduced by 84.98%, 85.24% and 64.02%, respectively. In the case of the inverter voltage all compensation methods achieved a fundamental component of 100% of its demanded value. In the case of the load current all compensation methods achieved very satisfactory results, however the exact compensation method was the most effective, achieving a load current of 99.11% of the expected value. The load current did not reach 100% of the expected value probably due to a small variation in the value of the 0.5 Ω load resistor.

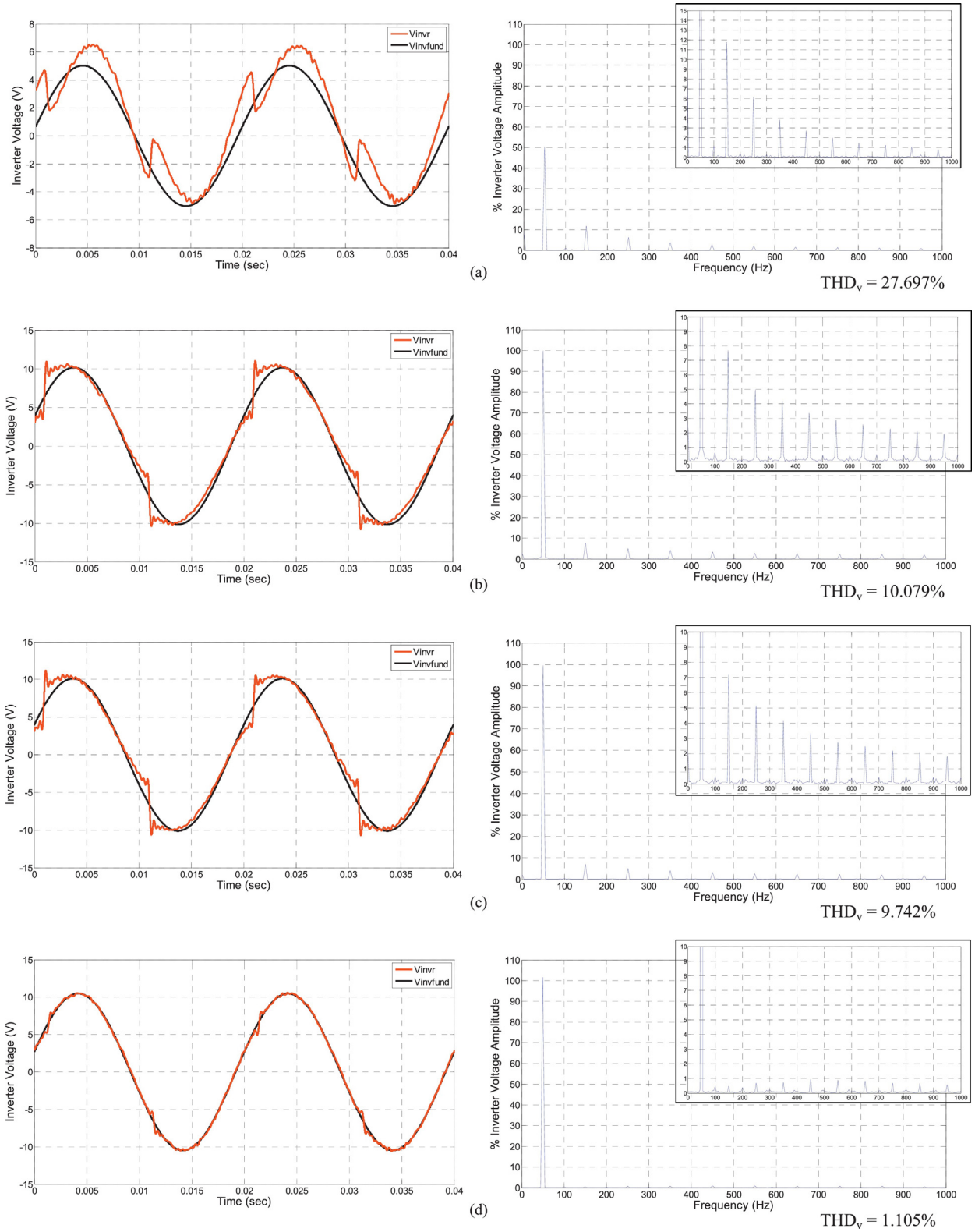


Fig. 19. Inverter voltage and voltage harmonic spectrum; (a) without compensation voltage, (b) with average voltage compensation, (c) with the voltage compensation calculated using the average load current, and (d) with the exact voltage compensation calculated using the instantaneous current (load resistance $R_L = 0.5\,\Omega$ and load inductance $L_L = 1.33\,\text{mH}$).

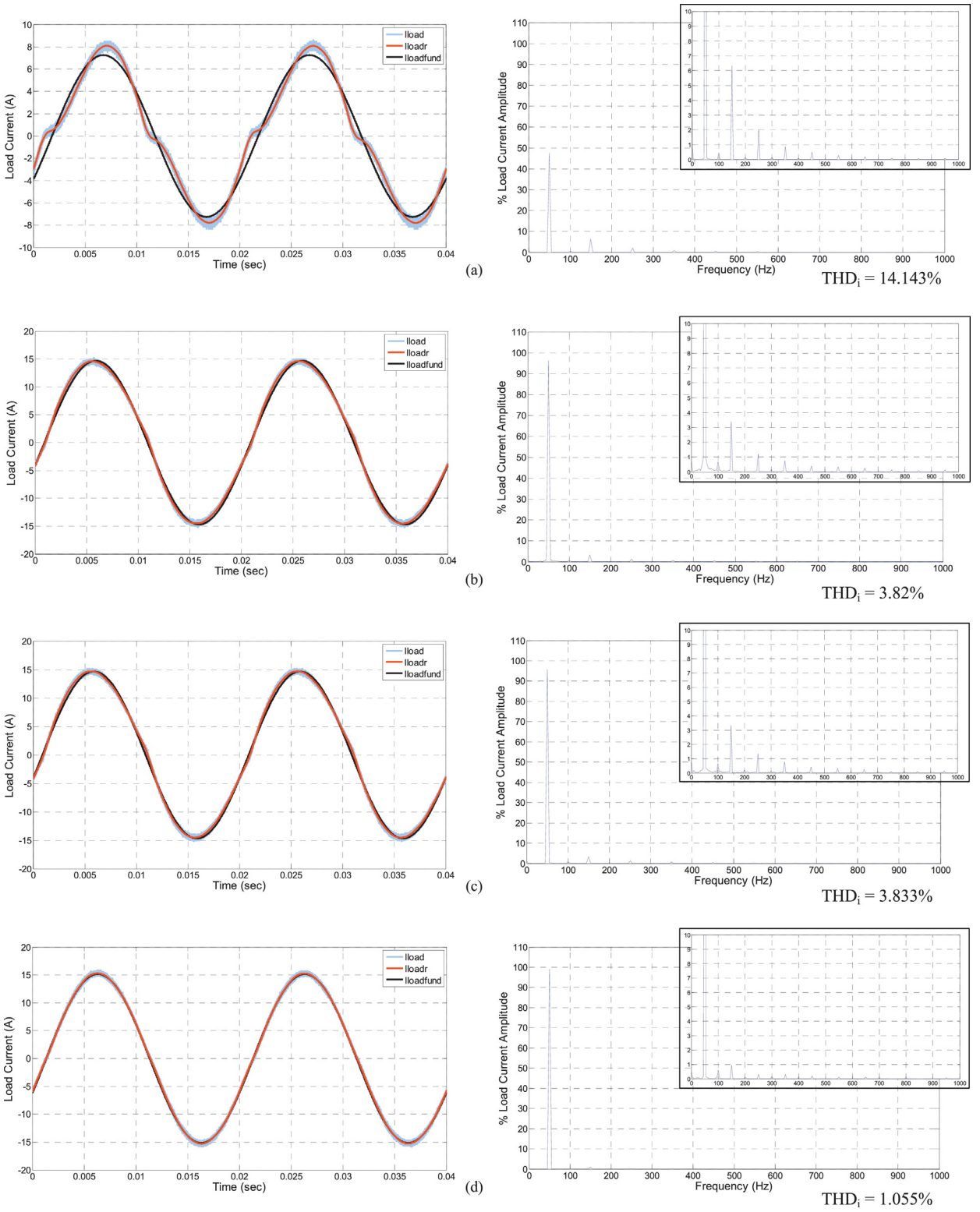


Fig. 20. Load current and current harmonic spectrum; (a) without compensation voltage, (b) with average voltage compensation, (c) with the voltage compensation calculated using the average load current, and (d) with the exact voltage compensation calculated using the instantaneous current (load resistance $R_L = 0.5\,\Omega$ and load inductance $L_L = 1.33$ mH).

7. Conclusion

This paper presented the effects of the non-linearities in an inverter on the output voltage and output current. The non-linearities caused by the dead time and by the voltage drops on the switching devices were discussed and the effects were observed from tests performed on a single phase inverter. Compensation techniques were formulated to compensate for these non-linearities. Novel compensation techniques that depend on the switching device current were formulated to compensate for the non-linearities in inverter circuits caused by the voltage drops on the switching devices. These compensation techniques were evaluated and tested by simulations and practical tests. All the three variations of the compensation technique provided very satisfactory results, however the exact compensation method was the most effective, achieving an inverter voltage fundamental component of 100% of its demanded value and a load current fundamental component of 99.11% of the expected value.

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