Ultra Low Frequency Low Power CMOS Oscillators for MPPT and Switch Mode Power Supplies

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***Abstract*—This paper presents the design of two low power consumption analog oscillators implemented in a $0.35\,\mu\mathrm{m}$ CMOS technology. These oscillators were designed for a power conditioning circuit with an analogue Perturbation and Observation (P&O) Maximum Power Point Tracker (MPPT) to maximize the scavenged power generated by energy harvesting devices. The nominal frequency of the two oscillators is $15\,\mathrm{Hz}$ and $200\,\mathrm{kHz}$, respectively. The $15\,\mathrm{Hz}$ oscillator is used to clock the MPPT, whereas the second oscillator generates a sawtooth wave required for the Pulse Width Modulation (PWM) of the switch mode converter. Both oscillators work with a supply voltage of $1\,\mathrm{V}$ and use a reference current generated by a self-biasing zero temperature coefficient circuit. All the circuitry was designed to operate in the sub-threshold region in order to keep its power consumption to a minimum. The frequency of the $15\,\mathrm{Hz}$ oscillator varies by $7.1\,\%$ over a temperature variation from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. The total power consumption including the current reference circuit is $30\,\mathrm{nW}$ at $27\,^{\circ}\mathrm{C}$ and reaches a maximum of $90\,\mathrm{nW}$ at $80\,^{\circ}\mathrm{C}$. The frequency of the $200\,\mathrm{kHz}$ oscillator varies by $33\,\%$ over a temperature variation from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$. The sawtooth generator, together with the current reference circuit, consume $63\,\mathrm{nW}$ across this temperature range.**

I. Introduction

Various applications require low frequency oscillators as part of their circuitry. Cardiac pacemakers, navy and submarine radio communication, MPPT circuits, sensor monitoring circuits, and low power switch mode converters all require a low frequency clock signal which has to be generated by ultra low frequency oscillators [1], [2].

The conventional CMOS ring oscillator generates a frequency in the order of MHz [3], [4]. To produce a lower frequency signal of the order of hundreds of Hz, frequency dividers have to be employed. Although this method is capable to accurately generate its designated frequency, its main drawback is the high static power consumption. Alternative circuit topologies, such as relaxation oscillators, exist but they are not capable of generating low frequency signals unless very large off-chip passive components are used [5].

An ultra low frequency ring oscillator using the concept of CMOS thyristors, was designed in [6]. The drawbacks of this oscillator are that it requires a minimum supply voltage of $2.5\,\mathrm{V}$, occupies a considerable area since it requires three capacitors and dissipates a static power of $5.7\,\mu\mathrm{W}$.

This paper presents the design of two low power consumption analog oscillators to be employed in a charge conditioning MPPT circuit for energy harvesting applications [2]. Both oscillators require only one capacitor and work with a supply voltage of $1\,\mathrm{V}$. Such a low supply voltage is beneficial so that the MPPT can operate once the voltage generated by the energy harvester exceeds $1\,\mathrm{V}$. The schematic diagram of the charge controller is shown in Fig. 1. The $15\,\mathrm{Hz}$ oscillator provides a clock signal to both a sample and hold (S&H) circuit and to a clocked comparator, which are essential to implement the P&O MPPT algorithm. The $200\,\mathrm{kHz}$ sawtooth generator is required to generate the PWM of an improved version dual boost converter, which is able to directly convert an AC input voltage to a DC output voltage without full wave rectification [7]. The power consumption of the sawtooth generator is very low and may also be used to generate PWM signals for other types of switch mode converters and power supplies. The frequency and duty cycle of the designed oscillators is controlled by means of a reference current, generated by a sub-threshold zero temperature coefficient self biasing circuit.

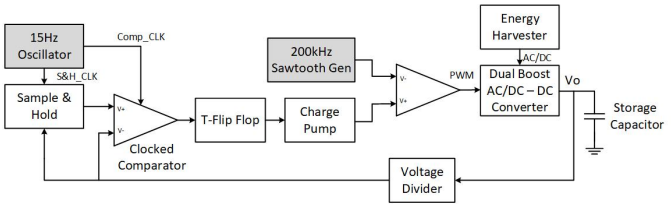

Fig. 1: Schematic diagram of the MPPT Charge Controller [2].

II. Design of the 15 Hz Oscillator

For the application described above [2], a low precision low power consumption oscillator is required. This oscillator is implemented by looping two Schmitt inverters to a current starved inverter, as shown in Fig. 2. It generates a clock signal of $15\,\mathrm{Hz}$. The current starved inverter charges and discharges the $1\,\mathrm{pF}$ timing capacitor *C1* and uses $1149\,\mu\mathrm{m}^2$ of area. The current which charges and discharges capacitor *C1* is set via two current mirrors.

The frequency and duty cycle of the generated clock pulses are determined by the current of the inverter, the capacitance of *C1* and the hysteresis values of the Schmitt inverter. The charging time of *C1* determines the clock pulse width, whereas the discharging time of *C1* determines the periodic time of the clock. In order for the clock frequency not to drift with temperature and voltage variations, a self biasing circuit generating a reference current was employed.

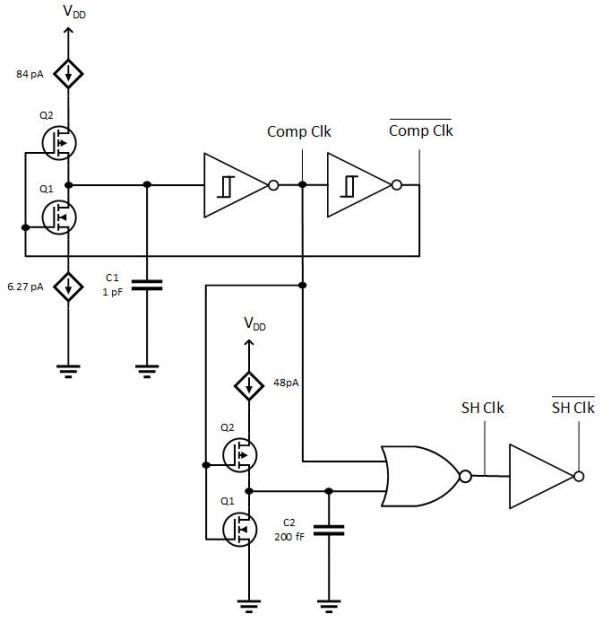

Fig. 2: 15 Hz MPPT Oscillator.

A zero temperature coefficient CMOS current reference circuit consisting of subthreshold transistors was designed [8]. This circuit consists of a self biased voltage reference subcircuit which generates the voltage V_{BIAS} to bias the current-source subcircuit. The former exhibits a positive temperature coefficient, whereas the current source subcircuit exhibits a negative temperature coefficient, resulting in a net zero temperature coefficient output current. Practical results show that this circuit consumes a power of $1\,\mu W$ [8]. The MPPT circuit without the reference current consumes $250\,nW$ [2] and therefore the reference current circuit proposed in [8] consumes too much power for this application. In order to consume less power, the circuit was modified as shown in Fig. 3. The bias-voltage subcircuit was redesigned to require only a self-biased Wilson current mirror [9]. To reach the required bias voltage for *Q9* with smaller currents, the diode connected transistor *Q3* was added. Analysis of this circuit yields:

$$I_O = I_{D_0} K_9 \left(\frac{K_1 K_{11}}{2 K_2 K_{10}} \right)^2 e^{\frac{2V_{GS3} + \delta V_{TH}}{n V_t}} \qquad (1)$$

where $\delta V_{TH} = V_{T_2} + V_{T_{11}} - V_{T_3} - V_{T_9} - V_{T_{10}}$ and K is the transistor aspect ratio.

From Eq. 1, it can be deduced that the thermal coefficient of the output current can be minimized through appropriate adjustment of the threshold voltages of *Q2, Q3, Q9, Q10* and *Q11*. This can be achieved by appropriate sizing. The reference current circuit designed for the oscillator consumes a power of $7.6\,nW$ at a temperature of $27\,^{\circ}C$. The current output variation with temperature is presented in Fig. 4.

The clock pulses supplied to the clocked comparator should be of at least $2\,ms$ for the comparator and the TFF to carry out their operation. The comparator is designed with low bias currents for minimal power dissipation resulting in a low slew

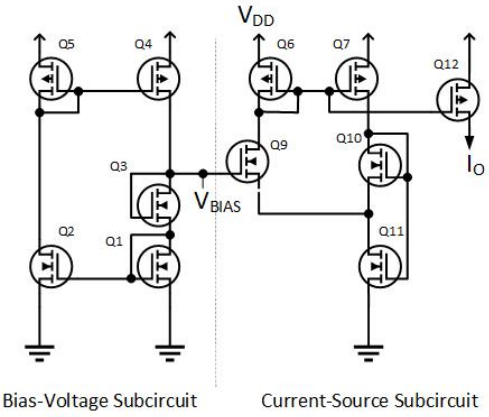

Fig. 3: Self-biasing temperature independent current reference circuit.

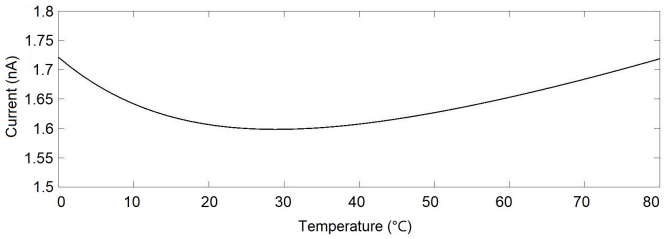

Fig. 4: Variation of the current reference output with temperature.

rate. In order to give allowance due to temperature and process variations, the oscillator was designed to have a pulse width of $5\,ms$. The hystheresis limits of the designed Schmitt inverter are of $180\,mV$ and $600\,mV$. Hence using $I = C\frac{\delta V}{\delta t}$ the charging current and discharging current are calculated to be $84\,pA$ and $6.27\,pA$, respectively.

This $15\,Hz$ oscillator also generates the clock pulses to the S&H circuit as shown in Fig. 1. This clock pulse is applied exactly once the comparator's clock pulse is over and should be of at least $500\,\mu s$ wide for the S&H's capacitor to charge or discharge to the input voltage.

This pulse is generated by the lower part of the circuit in Fig. 2. When Comp_Clk is at $1\,V$, capacitor *C2* discharges through transistor *Q1* and so the output of the NOR Gate which drives the S&H goes low. As soon as Comp_Clk is low, the NOR Gate's output goes high initiating the S&H clock pulse. Consequently, capacitor *C2* starts charging with a current of $48\,pA$ via another current mirror from the same reference current circuit. Once it charges to $340\,mV$, which is considered a high signal by the NOR gate, the NOR Gate's output goes back to low.

The Schmitt inverter, shown in Fig. 5, uses four stacked transistors to invert the input signal and two additional transistors, *Q5* and *Q6*, to feedback the output voltage [10] [11] to alter the threshold voltage of the inverter depending on the current state of the inverter. The aspect ratio of transistors *Q2* and *Q6* where adjusted to obtain the upper limit voltage (V_{IH}) required and the aspect ratio of transistors *Q5* and *Q4* was adjusted to achieve the lower limit voltage (V_{IL}) required.

The oscillator was simulated at various temperature con-

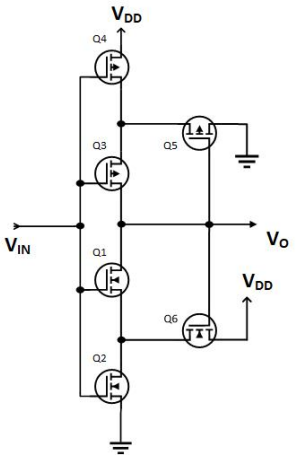

Fig. 5: The Schmitt Inverter.

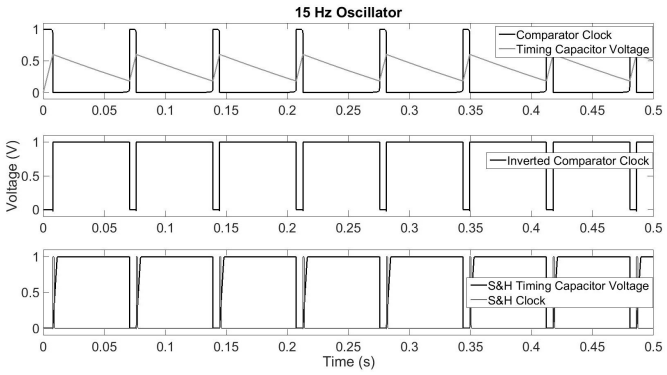

Fig. 6: 15 Hz Oscillator Timing Capacitors Voltages and Comparator and Sample & Hold Clock Pulses Plots

ditions. The results of the optimized design and its power dissipation (including reference current circuit) are listed in Table I. Corner analysis and Monte Carlo simulations were carried out to obtain a robust design. The frequency may drift from 14 Hz to 20 Hz when simulating with both temperature and process variations. Monte Carlo simulations resulted in a standard deviation of 6 Hz. The offset of the oscillator output frequency from the nominal 15 Hz are not expected to affect the operation of the MPPT circuit. Table II compares the performance of the proposed oscillator with the state of the art (SOA). The temperature coefficient and voltage coefficient of

TABLE I
PERFORMANCE OF THE 15 HZ OSCILLATOR ACROSS DIFFERENT TEMPERATURES.

Temp.	Frequency	Comp. Pulse	S&H Pulse	Cons.
0 °C	16 Hz	6.3 ms	1.5 ms	15 nW
27 °C	15 Hz	5.5 ms	1.2 ms	30 nW
80 °C	16 Hz	3.8 ms	0.8 ms	90 nW

TABLE II
COMPARISON OF THE 15 HZ OSCILLATOR WITH THE SOA.

Reference	Technology	Min. Supply Voltage	Frequency	Power
[1]	180 nm CMOS	2.5 V	0.303 Hz	6.6nW
[6]	250 nm CMOS	2.5 V	8.94 Hz	5.7 µW
[12]	2 µm CMOS	2 V	100 Hz	0.3 µW
This Work	0.35 µm CMOS	1 V	15 Hz	30nW

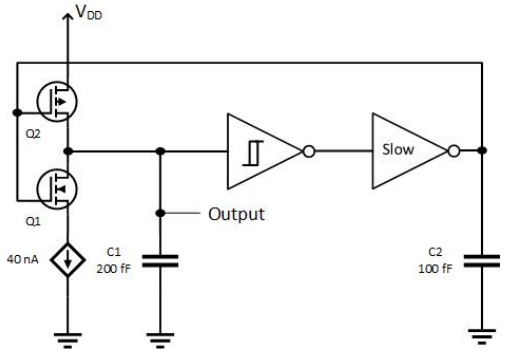

Fig. 7: 200 kHz Sawtooth Generator.

this oscillator are $0.27\,\%/°\mathrm{C}$ and $-0.069\,\%/°\mathrm{C}$ respectively. The area usage of this oscillator including the 200 fF capacitor required to generate the S&H clock pulse is of $1645\,\mu\mathrm{m}^2$.

III. DESIGN OF THE 200 KHZ SAWTOOTH GENERATOR

The sawtooth generator, shown in Fig. 7, is required to generate a PWM signal to control the switch mode boost converter. It generates a sawtooth waveform with a signal swing which goes from 0 V to 1 V at a frequency of 200 kHz. The circuit consists of a current starved inverter followed by a Schmitt inverter and a NOT gate designed to have a low output slew rate. The current starved inverter uses a current source in order to precisely control the rate at which the 200 fF timing capacitor *C1* is discharged.

The sawtooth output voltage wave is generated across the timing capacitor *C1*. The implemented Schmitt inverter circuit is shown in Fig. 5. It is designed to have a V_{IL} as close to 0 V as possible and, since the NOT gate has a low slew rate and a capacitive load of 100 fF, the current starved inverter would continue discharging capacitor *C1* for 50 ns after the Schmitt inverter changes its state. The timing capacitor is charged in 20 ns which is less than 1 % of the full cycle. Hence, the frequency of the oscillator is mainly determined by the discharging current, the timing capacitor and the hysteresis values of the Schmitt inverter, which are 0 V and 1 V.

A discharging current of 40 nA is required to achieve an oscillation frequency of 200 kHz. This current is set by mirroring a current from a self biased temperature independent reference current circuit, similar to the one shown in Fig. 3 and consumes 2.5 nW. It was ensured that the sawtooth waveform reaches the maximum value of the charge pump output voltage (1 V) at all operating temperatures and corner conditions, in order to prevent the output duty cycle from reaching 100%. Additionally, it was ensured that, across various process and temperature variations, the sawtooth generator does not have a dead band at 0 V, as this limits the lowest PWM duty cycle which can be obtained, thus limiting the operation of the boost converters at specific input and output voltages which require a low duty cycle. It is preferable that the sawtooth wave does not reach 0 V rather than having a dead-band at 0 V. The Schmitt inverter, similar to the one shown in Fig. 5, was designed to have $V_{IL} = 90\,\mathrm{mV}$ in typical conditions, by adjusting the aspect ratios of transistors *Q4* and *Q5*. V_{IH} was set to

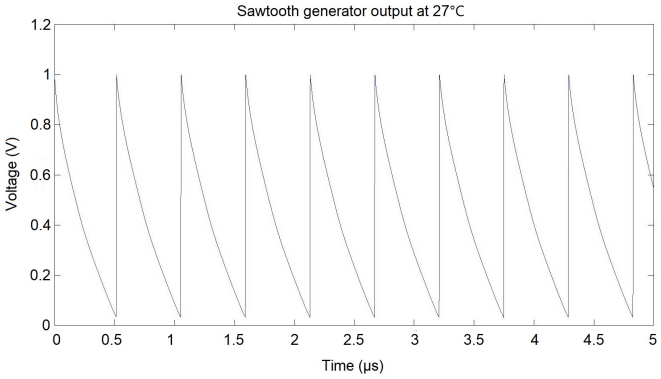

Fig. 8: Transient response of the Sawtooth Generator.

TABLE III
PERFORMANCE OF THE 200 KHZ SAWTOOTH OSCILLATOR ACROSS DIFFERENT TEMPERATURES.

Temp.	Frequency	Dead-band @ 0 V	Minimum Voltage	Maximum Voltage
0 °C	180 kHz	0 µs	10.7 mV	998 mV
27 °C	190 kHz	0 µs	37.5 mV	998 mV
80 °C	200 kHz	0 µs	80 mV	999 mV

800 mV in typical conditions. This was achieved by adjusting the aspect ratios of transistors *Q2* and *Q6*. The output of the sawtooth generator simulated at 27 °C with typical conditions is shown in Fig. 8.

The design of the oscillator was simulated and tested across various temperature conditions. The simulated results are presented in Table III, showing that no dead-band occurs neither at 1 V nor at 0 V. Corner analysis and Monte Carlo simulations were also carried out. Corner analysis with temperature variations resulted in the oscillator frequency to fluctuate from 140 kHz to 220 kHz. Monte Carlo simulations calculated a standard deviation of 34 kHz. Although the 200 kHz oscillator frequency is the ideal switching frequency for the boost converter in the MPPT circuit, variations in this frequency would only affect the switching losses and the ripple currents of the boost converter. The temperature coefficient and voltage coefficient of the proposed oscillator are 0.17 %/°C and 0.029 %/°C respectively and the circuit consumes an area of 436 µm^2. Table IV compares the specifications of the proposed oscillator with that of existing designs.

IV. CONCLUSION

Simulation results have shown that the frequency of the 15 Hz oscillator varies by 7.1 % over a temperature variation from −40 °C to 125 °C. The total power consumption, including that of the self-bias zero temperature coefficient current reference circuit, is 30 nW at 27 °C and reaches a maximum of 90 nW at 80 °C. The frequency of the 200 kHz sawtooth oscillator varies by 33 % over a temperature variation from −40 °C to 125 °C. The sawtooth generator together with the current reference circuit consume 63 nW, which remains constant throughout all temperature range. The variations due to temperature, in the sawtooth wave particularly the minimum voltage, as listed in Table III were found to be negligible and do not affect the operation of the switch mode converter and its controller.

TABLE IV
COMPARISON OF THE 200 KHZ OSCILLATOR WITH THE SOA.

Reference	Technology	Min. Supply Voltage	Frequency	Power
[5]	65 nm CMOS	1.5 V	18.5 kHz	120 nW
[13]	0.35 µm CMOS	1 V	80 kHz	1.14 µW
[14]	65 nm CMOS	1.05 V	100 kHz	41 µW
[15]	0.35 µm CMOS	1.2 V	200 kHz	84 µW
This Work	0.35 µm CMOS	1 V	200 kHz	63 nW

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