An Ultra Low Power CMOS MPPT Power Conditioning Circuit for Energy Harvesters

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Abstract—This paper presents the measured results and characterization of a fabricated power conditioning and energy storage integrated circuit for energy harvesters with on-chip maximum power point tracking (MPPT). This ultra-low power circuit employs an AC/DC-to-DC converter to be compatible with both AC and DC voltage energy harvesters, and features a wide input voltage and power range. The circuit was implemented using the AMS CMOS 0.35µm high voltage technology and all the circuit blocks were designed using analog electronic techniques, with the transistors operating in the sub-threshold region, in order to obtain a minimum power consumption. In fact, this power conditioning circuit consumes less than 2µW while featuring an input voltage range of ±0.5 V to ±50 V and a power range of 10µW to 200 mW.


I. INTRODUCTION

Energy harvesters are devices which harvest energy from their surroundings in order to power small loads. These devices eliminate the need of using batteries in applications where the battery longevity is an issue and battery replacement might not be feasible. A common disadvantage of energy harvesters is that their output is volatile and dependent on its current operating conditions. Thus, it is beneficial to have a power conditioning circuit to provide energy storage in order to minimize the downtime of the loads and a voltage regulation circuit to generate a constant output voltage. Energy harvesters also have an internal impedance and so it is beneficial for a power conditioning circuit to have a maximum power point tracking (MPPT) algorithm to match the load resistance to the internal impedance of the harvester by means of a switch-mode converter.

The power conditioning circuit proposed in [1] uses an AC/DC-to-DC converter so that whilst eliminating the losses incurred by a rectification block, it is still capable to work with both AC and DC energy harvesters. A block diagram of the power conditioning circuit is shown in Fig. 1. The first stage of the power conditioner consists of an AC/DC-to-DC converter controlled by an MPPT controller. Prototypes of this integrated circuit were fabricated and its measured results and characterization are being presented in this paper. The final stage of the power conditioner, the voltage regulating block, will be designed and fabricated at a later stage. The circuit is designed to work with a wide input voltage and power range which are ±0.5 V to ±50 V and 10µW to 200 mW respectively. This makes it compatible with solar cells, pyroelectric, thermo-electric, piezo-electric, electromagnetic and electrostatic energy harvesters.

Fig. 1: Block diagram of the proposed power conditioning circuit [1].

The circuit implementation of the perturbation and observation MPPT algorithm control for the AC/DC-to-DC converter is shown in Fig. 2 [1]. The circuit is implemented using the AMS CMOS 0.35µm high voltage technology and all the circuit blocks were designed in analog electronics, with the transistors operating in the sub-threshold region to guarantee a minimum power consumption. This circuit consumes a total power of less than 2µW.

Fig. 2: Circuit implementation of the perturbation and observation MPPT algorithm control for the AC/DC-to-DC converter [1].

The MPPT algorithm is implemented around a sample and hold circuit and a clocked comparator, and it operates at a clock frequency of 15 Hz. This MPPT control loop only requires a voltage feedback which eliminates the need of current sensing and a multiplier block, leading to a low power consumption [2], [3]. If the load current is either constant or changes at a rate slower than the MPPT clock frequency, maximum power transfer can still be obtained. Once the clocked comparator detects that the output voltage is decreasing, it changes the state of the toggle flip flop. The charge pump either continuously increases or decreases its output voltage depending on the state of the toggle flip flop.
The output voltage is the reference voltage for the pulse width modulation (PWM) generator and controls the duty cycle at which the converter is operated. A 200 kHz sawtooth generator is also integrated in the circuit which is required for the PWM generation, switching the transistors of the converter at this frequency.

II. LAYOUT CONSIDERATIONS OF THE AC/DC-TO-DC CONVERTER WITH MPPT CONTROL

Following the circuit design and simulation at various temperature, voltage and process conditions [1], [4], the layout of the circuit was carried out. The layout is shown in Figure 3 with all the respective blocks labelled. The layout includes four high voltage pads and sixteen low voltage pads as shown in Fig. 4. Most of these pads were included to increase the testability of the prototype circuit. Pads were included at the input and output of every block, so that each individual block could be monitored externally. The dimension of the integrated circuit, including the pads, is 1271 \( \mu \text{m} \) by 1347 \( \mu \text{m} \), that is an area of 1.7 \( \text{mm}^2 \). The active circuit covers an area of 0.11 \( \text{mm}^2 \).

Fig. 3: Layout of the AC/DC-to-DC converter with MPPT control.

Post-layout simulations were carried out in order to assess the effect of the pads on the total power consumption and the functionality of the circuit blocks. This was particularly relevant for those pads switching at a high frequency such as the sawtooth generator and gate driver pads, since pad loading tend to slow their response time. Although post layout simulations of the circuit with only the essential pads, showed that a static power consumption of 1.2 \( \mu \text{W} \) is demanded, this increases to 8.1 \( \mu \text{W} \) when all the pads are included since slight modifications to the circuitry had to be carried out, particularly the current biasing for the oscillators to maintain the designated oscillating frequency. The power consumption of the fabricated integrated circuit was measured to be 10 \( \mu \text{W} \) which is slightly higher than the consumption obtained in post layout simulations possibly because the sawtooth generator oscillated slightly higher than 200 kHz. However, if this circuit is fabricated without the redundant testing pads, the static power consumption is expected to drop back to below 2 \( \mu \text{W} \).

III. INTEGRATED ULTRA LOW FREQUENCY, LOW POWER OSCILLATORS

The low power consumption and ultra low frequency on-chip oscillators were designed by cascading and looping Schmitt inverters with a current starved inverter. The current starved inverter is biased from a temperature and voltage independent current reference circuit as shown in Fig. 5 and Fig. 6 respectively. The design of these circuits was reported in [4].

Fig. 4: Micro photograph of the fabricated integrated circuit.

Fig. 5: Simplified circuit diagram of the 15 Hz oscillator [4].

Fig. 6: Self-biasing temperature independent current reference circuit used to bias the current starved inverter [4].

Measured results obtained while testing the 15 Hz oscillator are shown in Fig. 7. A clock pulse is applied to the sample and hold circuit to store the current output voltage and after a
Fig. 7: Comparator (yellow) and sample & hold (blue) clock pulses generated by the 15 Hz oscillator.

short delay, a clock pulse is applied to the clocked comparator to compare the current output voltage to the previous output voltage. The measured frequency of the oscillator is 16.6 Hz, which is within the standard deviation of 6 Hz obtained in the Monte Carlo simulations [4]. The MPPT is still able to work at this clocking frequency. The sawtooth generator works on the same principle of the MPPT clock oscillator. Its simplified circuit diagram is shown in Fig. 8. Fig. 9 shows the measured sawtooth generator output oscillating at a frequency of 217 kHz. This frequency is also within the standard deviation of 34 kHz obtained in the Monte Carlo simulations [4].

Fig. 8: Simplified circuit diagram of the 200 kHz sawtooth generator [4].

IV. INTEGRATED IMPROVED DUAL BOOST CONVERTER

The AC/DC-to-DC converter topology chosen for this power conditioning circuit is the improved dual boost converter [5]. Further improvements were carried out on [5], in order to increase its operating efficiency. The gates of transistors $M_2$ and $M_3$ were connected to the same gate driver as shown in Fig. 11. This increased the efficiency of the converter for two reasons. Primarily, during the input positive half cycle, if only $M_3$ is switched on, the parasitic diode of $M_2$ needs to be forward biased which will eventually have a voltage drop $V_F$ of around 0.7 V. By switching $M_2$ and $M_3$ on simultaneously, instead of the voltage drop $V_F$, current is now limited by $R_{ON}$ only, which is estimated to be around $5 \, \text{m}\Omega$ when operated at a gate voltage of 2 V [6]. The measured PWM signal applied to the gates of the improved dual boost converter is shown in Fig. 10.

Similarly, the same improvement is obtained during the input negative half cycle when instead of switching on only $M_2$, both $M_2$ and $M_3$ are switched on simultaneously. Another advantage is that now the polarity sensing block is not required which further improves the efficiency of the control circuitry. A second improvement is that the two diode connected transistors were connected in parallel to transistors $M_2$ and $M_3$ as shown in Fig. 11. This further improves the efficiency of the converter during the off period because the conducting losses of an MOS parasitic diode is higher than that of a diode connected MOS transistor. The only off-chip components required by the power conditioning circuit are a $1 \, \text{mH}$ inductor and an output storage capacitor of $200 \, \text{pF}$, which are both required for the dual boost converter.

The improved dual boost converter was tested at fixed input voltage, output load and duty cycle conditions and some of the measured results are presented in Fig. 12. The input and output voltages together with the input current were recorded using the Keithley 2001 Precision Multimeter, which is capable of measuring currents as low as $10 \, \text{pA}$ [7]. The output current was estimated from the output voltage and the load resistance. A peak efficiency of 60.3% was measured.

Fig. 9: Measured results of the sawtooth signal generator.

Fig. 10: PWM output of the gate driving comparator, at a 50% duty cycle, being applied to the switching devices of the dual boost AC/DC-to-DC converter.

Fig. 11: Improved dual boost AC/DC-to-DC converter.
with the boost converter in operation and a peak efficiency of 95.2% when operated just as a rectifier. A maximum boosting ratio of 570% was obtained at continuous conduction mode (CCM) operation. A higher ratio is obtained at discontinuous conduction mode (DCM) operation.

Table I compares the measured performance of the converter designed within the proposed architecture with the state-of-the-art (SOA) of AC-DC converters designed for energy harvesters. The efficiency levels obtained compare with those of other converters but the featured input voltage and power range of the proposed converter is much wider and so it can be used with a wider range of energy harvesters. The circuit presented in [8] has a wide input voltage range of up to ±40 V, but this converter is not integrated since its transistors and passive components are all externally connected.

### V. Integrated Efficient Voltage Divider

The AC/DC-to-DC converter output can charge the storage capacitor up to a maximum voltage of 50 V. However, the control circuitry works with a supply voltage of 1 V and control signal voltages within 0 V to 1 V. Therefore to adequately sense the output voltage, a voltage divider is required to reduce this voltage by a factor of 50. Large resistors consume a very large area in an integrated circuit. Since the voltage across the voltage divider can reach 50 V, the power dissipation by the voltage divider having a total resistance of 200 kΩ was estimated to be in the mW range. As a solution an innovative voltage divider using transistors in the cut-off region is shown in Fig. 13. Simulation results showed that the power dissipation at an input voltage of 50 V is of 7.1 nW.

A capacitive voltage divider was paralleled with the resistive voltage divider to improve its response time. Fig. 14 shows the measured output voltage and input current at various input voltage conditions. The voltage divider was tested up to a 25 V input voltage. The measured voltage division factor of 50, corresponds to that obtained in the simulations. However, the measured power consumption of the voltage divider reached 1.7 µW at an output voltage of 25 V. This needs further investigation because there is a large discrepancy from the 7.1 nW consumption obtained in the simulations. Nonetheless, this is still substantially lower from implementing the voltage divider using the resistors available in the employed technology.

### VI. Conclusions and Further Work

This paper presented the measured results of some of the main circuit blocks implemented in the AC/DC-to-DC converter with MPPT algorithm. These results show that the novel circuitry implemented in this power conditioning circuit works as predicated by the simulations. If this circuit is fabricated without the testing pads, the static power consumption is expected to be less than 2 µW. The integrated AC/DC-to-DC converter works as expected with a peak efficiency of 60%. The power conditioning integrated circuit will be further tested with different energy harvesters in order to confirm its MPPT operation over various input and load conditions. Eventually, the design and fabrication of the voltage regulating DC-DC converter will be carried out. This is to be connected to the output of the AC/DC-to-DC converter with MPPT control, in order to generate a constant output voltage.
REFERENCES


