



L-Università
ta' Malta

MATSEC
Examinations Board



Marking Scheme

AM07 Computing

Main Session 2019

Marking schemes published by the MATSEC Examination Board are not intended to be standalone documents. They are an essential resource for markers who are subsequently monitored through a verification process to ensure consistent and accurate application of the marking scheme.


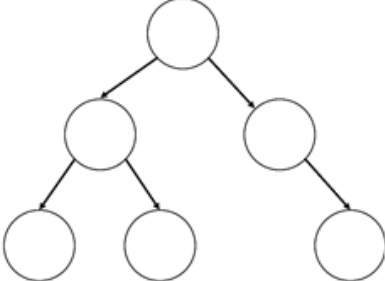
In the case of marking schemes that include model solutions or answers, it should be noted that these are not intended to be exhaustive. Variations and alternatives may also be acceptable. Examiners must consider all answers on their merits, and will have consulted with the MATSEC Examinations Board when in doubt.

Paper I

Question		Answer	Mark
1	a	6 8 7 5 9	1
		6 7 8 5 9	1
5 6 7 8 9		1	
5 6 7 8 9		1	
	b	Insertion sort	1
Total:			5
2	a	Overriding	1
	b	20,000	1
	c	40,000	1
	d	No.	1
In order for ComputerEngineer to correctly override the printSalary() method, it needs to have the same level of visibility as in the superclass.		1	
Total:			5
3		Packet Switching	1
		Circuit Switching	1
		Message Switching	1
		Packet switching: message is divided into blocks called packets which are sent over the network. Circuit switching: network establishes a fixed bandwidth circuit between nodes before user communicates. Message switching: whole message is sent in one go.	1 each for any two
Total:			5
4	a	It should be 0.	1
		In this way there are an even number of 1s in the transmission.	1
	b	If there was an error in transmission, the number of 1s would be odd.	1
	c	Stop and Wait	1 each for any two
		Go Back N Selective Repeat	
Total:			5
5	a	Handshaking occurs when two unsynchronized devices would like to send data to each other	1
		The sender sends data to the receiver and waits for an acknowledgement <i>When the acknowledgement is received, the sender starts sending the data.</i>	1 1

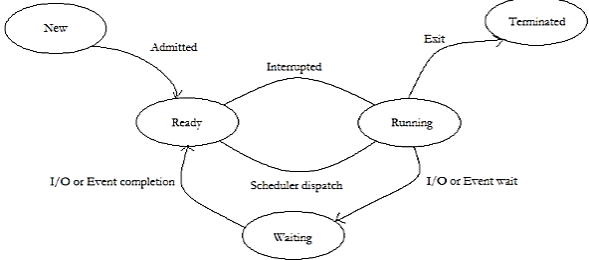
	b	Round robin Shortest job first Priority based First-in first-out	1 each for any two
Total:			5
6	a	This is useful to prevent processes from accessing storage allocated to other jobs.	1
	b	Storage space ends up “wasted” Reading/writing is slower Data corruption or data loss Computer system crashes or freezes	1 each for any two
	c	The disjoint blocks are physically moved around such that they are now one after another. The free space now consists of a large single block.	1 1
Total:			5
7	a	No action is taken.	1
	b	<pre> graph TD Begin([Begin]) --> Salary{Salary Due?} Salary -- YES --> PaySalary[Pay Salary] PaySalary --> Overtime{Overtime worked?} Overtime -- YES --> PayOvertime[Pay overtime] PayOvertime --> End([End]) Salary -- NO --> End Overtime -- NO --> End </pre>	4
Total:			5
8	a	Adaptive maintenance Modifying the system to cope with changes in the software environment. Corrective maintenance Diagnosing and fixing errors, possibly ones found by users. Perfective maintenance Implementing new or changed user requirements which concern functional enhancements to the software. Predictive maintenance	2 each for any two

		Increasing software maintainability or reliability to prevent problems in the future.	
	b	Involves many groups of users whose responsibilities cross traditional department or division boundaries Is considered critical to the future success of the organization Is a first-time project for the organization	1 for any one
Total:			5
9	a	Technical Operational Timeliness Economic Legal Social	1 each for any two
	b	Problem identification System analysis / requirement analysis System design Implementation Testing Maintenance Evaluation	1 each for any three
Total:			5
10	a	$\langle letter \rangle ::= "A" \mid "B" \mid "C" \mid \dots \mid "Z"$ $\langle digit \rangle ::= "0" \mid "1" \mid \dots \mid "9"$ $\langle product\ code \rangle ::= \langle letter \rangle \langle digit \rangle \langle digit \rangle \langle letter \rangle \langle letter \rangle \langle letter \rangle$	4
	b	EBNF is an extension of BNF	1
Total:			5
11	a	The table should be in the 2NF	1
		Every non-prime attribute of the table is non-transitively dependent on every key of the table	1
	b	Primary key: a key which is a unique identifier for each record (row) Foreign key: a field in one table which uniquely identifies a row in another table Attribute: a column in a particular database table	1 1 1
Total:			5
12	a	name surname Anthony Attard Corinne Camilleri	2
	b	data consistency portability control over redundancy protection against unauthorized access	1 each for any two

		greater complexity vulnerability to system failure vulnerability to unauthorized access	1 for any one																																																																																										
Total:			5																																																																																										
13	a	[10], no returned value [15, 10], no returned value [10], returned value = 15 [20, 10], no returned value	1 1 1 1																																																																																										
	b	A static stack structure does not change, while a dynamic stack structure can be changed depending on the operations performed.	1																																																																																										
Total:			5																																																																																										
14	a	 	2 2																																																																																										
	b	A hash function maps a key to a hash value to index and locate entries in a hash table.	1																																																																																										
Total:			5																																																																																										
15	<p>Using truth tables:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>$\bar{A}\bar{B}\bar{C}$</th> <th>BC</th> <th>LHS</th> <th>$\bar{A}+B$</th> <th>$B+\bar{C}$</th> <th>$\bar{B}+C$</th> <th>RHS</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> <p>LHS = RHS</p> <p>Or using Boolean algebra:</p> $ \begin{aligned} (\bar{A} + B)(B + \bar{C})(\bar{B} + C) &= (\bar{A} + B)(B\bar{B} + BC + \bar{B}\bar{C} + \bar{C}C) \\ &= (\bar{A} + B)(BC + \bar{B}\bar{C}) \\ &= \bar{A}BC + \bar{A}\bar{B}\bar{C} + BBC + B\bar{B}\bar{C} \\ &= \bar{A}BC + \bar{A}\bar{B}\bar{C} + BC \\ &= BC(\bar{A} + 1) + \bar{A}\bar{B}\bar{C} \\ &= BC + \bar{A}\bar{B}\bar{C} \end{aligned} $ <p>If some other method is used that demonstrates the equality, it should be accepted.</p>		A	B	C	$\bar{A}\bar{B}\bar{C}$	BC	LHS	$\bar{A}+B$	$B+\bar{C}$	$\bar{B}+C$	RHS	0	0	0	1	0	1	1	1	1	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	1	0	1	1	0	0	0	0	1	1	0	0	1	1	1	0	1	1	1	1	1	1	5
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Total:			5																																																																																										

16	a	0101.1010	1
	b	5.625	1
	c	1011.1100	1
	d	$11.75 - 16 = -4.25$	2
Total:			5
17	a	4	1
	b	7	2
	c	5	2
Total:			5
18	a	The interrupting device sends an id, and the processor uses the id to determine the interrupt service routine to execute.	2
	b	There is a single interrupt single service routine which polls all the devices to determine which device triggered the interrupt.	2
	c	Vectored interrupts are faster.	1
Total:			5
19	a	Serial transmission. Advantage: e.g. no need to synchronize the parallel lines.	2
	b	Asynchronous. Advantage: e.g. the clock does not need to have the same frequency as the host computer's.	2
	c	Connecting storage devices, keyboard, mouse, etc. Simple charging is not a good answer, as it does not use USB communication.	1
Total:			5
20		14	5
Total:			5

Paper II

Question		Answer	Mark	
1	a		6	
	b	<p>Contiguous blocks would be the best. This is simpler than linked or indexed blocks. Damage to a single block will not affect other blocks as in linked or indexed blocks.</p>	1 1 1	
	c	<p>Thrashing occurs when the CPU spends most of its time swapping pages rather than doing productive work. Thrashing can be avoided by setting a limit on the number of possible active processes.</p>	2 1	
	d	<p>Users submit jobs to the batch OS. The jobs are batched and are processed in one go. When the job finishes executing, its memory is released and the output for the job gets copied into an output spool for later printing or processing.</p>	2 2 2	
	e	<p>Online Real-time Network Time-sharing</p>	1 each for any two	
Total:			20	
2	a	<p>Analogue signals vary continuously in time, and have properties such as amplitude, phase and frequency. Digital signals vary discretely in time between two values e.g. 1 and 0.</p>	3 3	
	b	<p>Multiplexing involves combining several signals and transmitting them over a single channel. In TDM, each user is assigned a timeslot in which to transmit data. In FDM, each user transmits on a different frequency</p>	2 2 2	
	c	i	<p>Star topology This meets company's requirement that all packets pass through the main server.</p>	1 2
		ii	<p>A disadvantage is that if the central node fails, the whole network goes down.</p>	3
		iii	<p>LAN LANs are suitable for use within a single building</p>	1 1
Total:			20	

3	a	Drawing seller	1																					
		Drawing shopper	1																					
		Log in	1																					
		Make purchase	1																					
3	c	View products	1																					
		Post advert	1																					
		Appropriate connections	2																					
		Prototyping refers to a first draft of a product which can be tested in a controlled environment prior to building the finished product.	2																					
3	d	Problem Identification	1																					
		Requirements Analysis	1																					
		System Design	1																					
		Feasibility Study	1																					
		RAD is incremental and iterative	1																					
		Waterfall is linear and predictive	1																					
3	d	RAD is ideal for short duration projects	1																					
		Waterfall is ideal for medium to long duration projects	1																					
		RAD testing is performed at every iteration	1																					
		Waterfall method testing is only performed after the system implementation phase.	1																					
		Total:			20																			
		4	a	Table is already in 1NF (contains atomic values)	4																			
2NF:	4																							
<table border="1"> <thead> <tr> <th>Supplier code</th> <th>Product code</th> <th>Quantity</th> </tr> </thead> <tbody> <tr> <td>DX15</td> <td>PR1</td> <td>250</td> </tr> <tr> <td>DX15</td> <td>PR2</td> <td>150</td> </tr> <tr> <td>QP07</td> <td>PR1</td> <td>350</td> </tr> <tr> <td>DX15</td> <td>PR3</td> <td>200</td> </tr> <tr> <td>QP07</td> <td>PR2</td> <td>200</td> </tr> <tr> <td>QP07</td> <td>PR3</td> <td>250</td> </tr> </tbody> </table>	Supplier code			Product code	Quantity	DX15	PR1	250	DX15	PR2	150	QP07	PR1	350	DX15	PR3	200	QP07	PR2	200	QP07	PR3	250	
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		QP07	PR1	350	
		DX15	PR3	200	
		QP07	PR2	200	
		QP07	PR3	250	
	b	Naming and discussing any two of the following: HR (e.g. employee information) Commercial (e.g. products) Education (e.g. schools) Health (e.g. medical records) etc			2 each for any two
	c	Naming and discussing any two of the following: Flat files Hierarchical Network Relational Object-oriented			2 each for any two
				Total:	20
5	a	int floorNumber = 5; Correct data type Correct variable name			1 1
	b	A new class called Villa can be created Villa should extend Property			1 1
	c	House house = new House(); house.updateNumberOfBathrooms(2);			4
	d	Inheritance is used in Apartment extends Property Inheritance is used in House extends Property Information hiding is used in private int price in Property Information hiding is used in private boolean isServicedByLift in Property			1 1 1 1
	e	It provides a clear modular structure for programs which makes it good for defining abstract datatypes in which implementation details are hidden. Objects can also be reused within an across applications. The reuse of software also lowers the cost of development. More effort is put into the object-oriented analysis and design, which lowers the overall cost of development. It makes software easier to maintain. Since the design is modular, part of the system can be updated in case of issues without a need to make large-scale changes			2 each for any two

		Reuse also enables faster development. Object-oriented programming languages come with rich libraries of objects, and code developed during projects is also reusable in future projects. It provides a good framework for code libraries where the supplied software components can be easily adapted and modified by the programmer. This is particularly useful for developing graphical user interfaces.	
	f	i The throws keyword indicates that a method may cause a particular exception at run time	2
		ii "Exception caught!" "Final block"	1 1
Total:			20
6	a	The processor determines the instruction address using the program counter (PC), which is then incremented to point to the next instruction. Then the processor sets the MAR to the instruction address and starts a read operation. The instruction is then read into the MDR. The instruction is transferred from the MDR to the CIR and decoded. Then the instruction is executed, for example an arithmetic operation will be executed by the ALU.	2 2 2 2
	b	push: no jc: yes call: yes stc: no	½ if not stated ½ if stated ½ if stated ½ if not stated
	c	The processor sets the address line to the address of the required memory location. The write enable line is not asserted, as this is a read operation. The memory device then sets the data bus to the value of the memory contents at the specified location, and the processor reads the data from the data lines.	1 1 2
	d	i around 4000 Mb, or 4096 Mb, or 4 Gb, or 2 ³² bytes	3
		ii around 3500 Mb	1
		iii around 12.5%	2
Total:			20
7	a	97, 76, 40	2
	b	97, 76, 40; 97, 83, 40; 97, 83, 76	7
	c	97, 83, 76	2
	d	It inserts the value of ax into the dx (3 in the run above) bytes starting at bx keeping them in descending order.	3
	e	i Two more element should be initialized, dx must be set to 5.	1
		ii No changes.	2
f	Register addressing: e.g. mov ax, cx Immediate addressing: e.g. mov ax, 76 Indexed addressing: mov [bx + di], ax	3	
Total:			20

		<table border="1"> <thead> <tr> <th>A_3</th> <th>A_2</th> <th>A_1</th> <th>A_0</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>X</td></tr> </tbody> </table>	A_3	A_2	A_1	A_0	F	0	0	0	0	X	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0	1	1	0	X	0	1	1	1	1	1	0	0	0	1	1	0	0	1	1	1	0	1	0	1	1	0	1	1	1	1	1	0	0	1	1	1	0	1	0	1	1	1	0	X	1	1	1	1	X	3
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	c	<p>Some variation is of course allowed as long as the result is the same.</p>	8																																																																																					
	d	NOR Gate.	1																																																																																					
	e	$\overline{XY + \bar{X}Y\bar{Z}} = \overline{Y(X + \bar{X}\bar{Z})}$ $= \overline{Y(X + \bar{Z})}$ $= \overline{XY + Y\bar{Z}}$ $= \overline{\bar{X}Y\bar{Z}}$	3																																																																																					
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