L-Università ta' Malta

MATSEC
Examinations Board

Marking Scheme

AM Computing

Special September Session 2020

Marking schemes published by the MATSEC Examination Board are not intended to be standalone documents. They are an essential resource for markers who are subsequently monitored through a verification process to ensure consistent and accurate application of the marking scheme.

In the case of marking schemes that include model solutions or answers, it should be noted that these are not intended to be exhaustive. Variations and alternatives may also be acceptable. Examiners must consider all answers on their merits, and will have consulted with the MATSEC Examinations Board when in doubt.

PAPER 1

Question			Suggested Answer	Marks Distribution	Marks
1	a		Second Result.		1
	b		The output is “Second Result” followed by “Third Result”.		2
	c		If no preceding case statements are matched, the default statement is entered.		2
				Total:	**5**
2	a		**** *** **	1 1 1	3
	b	i	Int or any other suitable numeric database.		1
		ii	Boolean.		1
				Total:	**5**
3	a		A public key is only used to encrypt the message, and can be sent to others. A private key is used to both encrypt and decrypt messages, and should never be shared.	1 1	2
	b		`2^128 or 3.4E38` possible addresses.		1
	c		Ring, mesh, star, bus or point-to-point. A correct description of the selected topology.	1 mark for any one 1	2
				Total:	**5**
4	a		It is used to transmit multiple signals over the same channel.		1
	b		Time Division Multiplexing. Time Division Multiplexing, each sender is assigned a time slot in which to transmit data. Frequency Division Multiplexing. Frequency Division Multiplexing, each sender is assigned a different frequency.	1 1 1 1	4
				Total:	**5**
5	a		ISR is a software process invoked by an interrupt request from a hardware device. It handles the request and sends it to the CPU, interrupting the active process. When the ISR is complete, the process is resumed.		2
	b		The stack is used to save the contents of the CPU registers before the interrupt is handled, and then the contents are popped back into the register.		2
	c		Contiguous, linked or indexed.		1
				Total:	**5**
6	a		Memory fragmentation occurs when memory is allocated in a large number of non-contiguous blocks, leaving a large percentage of memory unallocated.		1
	b		Technique is called compaction. Compaction fixes fragmentation by moving all allocated blocks to one end of memory, leaving a larger free space.	1 2	3

<table>
<tr><td></td><td>c</td><td></td><td>User ID and password, file access rights, access by location.</td><td></td><td>1</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
<tr><td>7</td><td>a</td><td></td><td>Microsoft Access or Delphi.</td><td></td><td>1</td></tr>
<tr><td></td><td>b</td><td>i</td><td>Stating any of Employee ID, Name, Surname or Salary.</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>ii</td><td>Stating a record such as 1750 Matthew Xuereb 25,000.</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>iii</td><td>Employee ID, because it is guaranteed to be unique.</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>iv</td><td>1938 Francesca Attard 26,000.</td><td></td><td>1</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
<tr><td>8</td><td>a</td><td></td><td>Naming and briefly describing (typically in one sentence) any three of the following: network, relational, flat, hierarchical, object-oriented.</td><td>1 mark each for any three</td><td>3</td></tr>
<tr><td></td><td>b</td><td></td><td>A secondary key is a non-unique attribute, which may be used to find row(s) in a table.</td><td></td><td>2</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
<tr><td>9</td><td>a</td><td>i</td><td>queue or FIFO</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>ii</td><td>stack or LIFO</td><td></td><td>1</td></tr>
<tr><td></td><td>b</td><td></td><td>A valid sorting algorithm.
Demonstrating knowledge of how the list would be sorted.</td><td>1
2
Deduct 1 mark for incorrect sorting</td><td>3</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
<tr><td>10</td><td>a</td><td></td><td>A pointer stores the address in memory of a data structure.</td><td></td><td>1</td></tr>
<tr><td></td><td>b</td><td></td><td>A static structure does not change in size.
Dynamic structure changes in size.</td><td>1
1</td><td>2</td></tr>
<tr><td></td><td>c</td><td></td><td>Either of linear search or binary search.
At least a one sentence valid description of how the algorithm works.</td><td>1
1</td><td>2</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
<tr><td>11</td><td>a</td><td>i</td><td>11111_2</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>ii</td><td>$2^5-1=31$</td><td></td><td>1</td></tr>
<tr><td></td><td>b</td><td></td><td><table><tr><th>A</th><th>B</th><th>C</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td></tr></table></td><td>1 mark for correct truth table format

2 marks for correct Y output</td><td>3</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
<tr><td>12</td><td>a</td><td>i</td><td>1001</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>ii</td><td>0011</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>iii</td><td>1100</td><td></td><td>1</td></tr>
<tr><td></td><td>b</td><td></td><td>overflow</td><td>An explanation should be included</td><td>2</td></tr>
<tr><td colspan="5">Total:</td><td>5</td></tr>
</table>

13	a		Dynamic RAM volatile while Static RAM non-volatile. Static RAM is faster than Dynamic RAM. Dynamic RAM takes less physical area than Static RAM. (Also accept DRAM can have larger size than SRAM).	1 1 1	3
	b		Example of DRAM – Computer Memory. Example of SRAM – CPU Cache.	1 1	2
				Total:	**5**
14	a		RISC – Reduced Instruction Set Computer. CISC – Complex Instruction Set Computer.	1 1	2
	b		CISC has a large set of instructions when compared to RISC. RISC has a larger amount of registers than CISC. CISC instruction sets are of variable format when compared to RISC.	1 mark each for any two	2
	c		Greater performance due to reduced instruction set and simpler architecture. Smaller in size than their CISC counterparts. Cheaper in cost.	1 mark each for any one	1
				Total:	**5**
15	a		Accept as answer 2^8=256 addresses		2
	b		15-bits	1 mark for correct answer. 2 marks for working.	3
				Total:	**5**
16	a		Accept as answer the following, or similar: While both compilers and interpreters convert a high-level language to machine language, an … …interpreter converts the program line-by-line during runtime. On the other hand, the compiler converts the whole program and generates an executable… … An assembler converts only an assembly program to machine language.	 1 1 1	3
	b		Accept as examples for compiled languages – C, C++ Accept as examples for interpreted languages – Python, Ruby, Matlab.	1 1	2
				Total:	**5**
17	a		BNF – Backus Naur Form. EBNF – Extended Backus Naur Form.	1 1	2
	b		A debugger is used to identify any coding errors during software development.	1 mark for definition of debugger 1 mark for identification of stage	2
	c		The syntax of a language refers to its form whist the semantics refers to its meaning.		1
				Total:	**5**
18			Problem Definition	5 marks if	5

<table>
<tr><td></td><td></td><td></td><td>Feasibility Study
Requirements Elicitation
Analysis
Design
Implementation
Testing
Maintenance
Retirement</td><td>complete

Deduct 1 mark if there is a slight deviation in the answers but the most important steps are included.

Accept minor variation in terms since stages' names vary from one textbook to another</td><td></td></tr>
<tr><td colspan="4"></td><td>Total:</td><td>5</td></tr>
<tr><td rowspan="2">19</td><td>a</td><td></td><td>Black box testing is functional testing where various inputs are inserted and the behaviour of the system is monitored, whereas white box testing is more logically based that examines the internal structure of the system.</td><td></td><td>3</td></tr>
<tr><td>b</td><td></td><td>White box testing is more effective because it tests the internal operation of the system.</td><td></td><td>2</td></tr>
<tr><td colspan="4"></td><td>Total:</td><td>5</td></tr>
<tr><td>20</td><td>a</td><td></td><td>Contents of EX after execution = 21.</td><td></td><td>3</td></tr>
<tr><td></td><td>b</td><td></td><td>Fibonacci Sequence Generator.

<table>
<tr><th>Iteration No.</th><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>AX</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CX</td><td>1</td><td>2</td><td>3</td><td>5</td><td>8</td><td>13</td><td>21</td><td>34</td></tr>
<tr><td>DX</td><td>1</td><td>2</td><td>3</td><td>5</td><td>8</td><td>13</td><td>21</td><td>34</td></tr>
<tr><td>EX</td><td>1</td><td>1</td><td>2</td><td>3</td><td>5</td><td>8</td><td>13</td><td>21</td></tr>
</table></td><td>1 mark for correct value of EX.

1 mark for correct answer to the program application.</td><td>2</td></tr>
<tr><td colspan="4"></td><td>Total:</td><td>5</td></tr>
</table>

PAPER 2

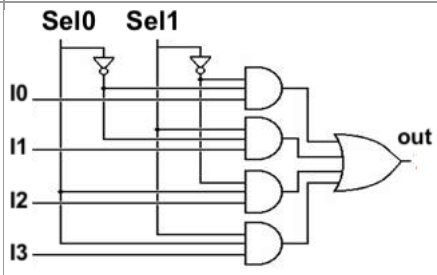
<table>
<tr><th colspan="3">Question</th><th>Model Answer</th><th>Marks Distribution</th><th>Marks</th></tr>
<tr><td>1</td><td>a</td><td></td><td>2 bits</td><td></td><td>2</td></tr>
<tr><td></td><td>b</td><td></td><td>
<table>
<tr><th>Sel_1</th><th>Sel_2</th><th>Out</th></tr>
<tr><td>0</td><td>0</td><td>I_0</td></tr>
<tr><td>0</td><td>0</td><td>I_1</td></tr>
<tr><td>1</td><td>0</td><td>I_2</td></tr>
<tr><td>1</td><td>1</td><td>I_3</td></tr>
</table>

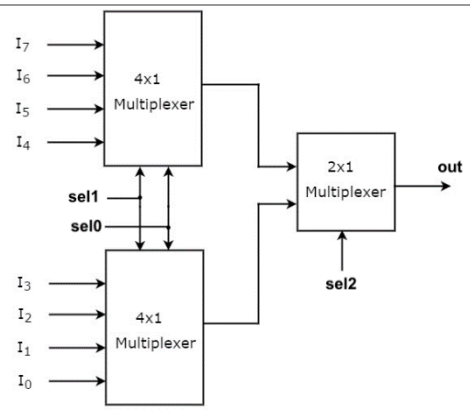
$out=sel_1.sel_2.I_0+sel_1.sel_2.I_1+sel_1.sel_2.I_2+sel_1.sel_2.I_3$

Note: There is another method to obtain the truth table, which is equally valid, but more complicated.</td><td>1 mark for each correct output value.

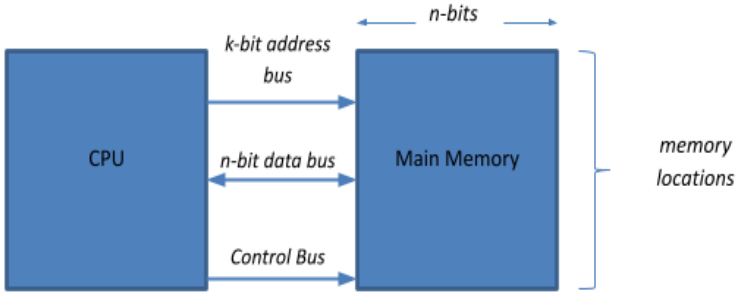
1 mark for correct input values.

3 marks for correct logic equation.

1 mark if the truth table is wrong but the logic expression corresponds to the truth table.</td><td>8</td></tr>
<tr><td></td><td>c</td><td></td><td> 
</td><td>5 marks for correct logic circuit.

3 marks if the logic circuit is incorrect but corresponds to the answer in b.</td><td>5</td></tr>
<tr><td></td><td>d</td><td></td><td> 
</td><td>5 marks for correct block diagram.

4 marks if sel^2 is missing.</td><td>5</td></tr>
<tr><td colspan="5">Total:</td><td>20</td></tr>
<tr><td>2</td><td>a</td><td>i</td><td>JGE LOOP</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>ii</td><td>HALT</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>iii</td><td>SUB AX, BX</td><td></td><td>1</td></tr>
<tr><td></td><td></td><td>iv</td><td>Any mnemonic from the code (MOV, JMP, SUB, INC, CMP, JGE)</td><td></td><td>1</td></tr>
<tr><td></td><td>b</td><td></td><td>14 iterations (answer in table below)</td><td>Working is expected by</td><td>6</td></tr>
</table>

			<table><tr><th>Iteration No.</th><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th></tr><tr><td>AX</td><td>100</td><td>93</td><td>86</td><td>79</td><td>72</td><td>65</td><td>58</td><td>51</td><td>44</td><td>37</td><td>30</td><td>23</td><td>16</td><td>9</td><td>2</td></tr><tr><td>BX</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td><td>7</td></tr><tr><td>CX</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td></tr></table>	performing a dry run. This will be useful for the subsequent answer.	
	c		`AX = 2, BX = 7, CX = 14`	No marks awarded for correct BX as it does not change.	2
	d		10 iterations (answer in table below) <table><tr><th>Iteration No.</th><th></th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th></tr><tr><td>AX</td><td>100</td><td>90</td><td>80</td><td>70</td><td>60</td><td>50</td><td>40</td><td>30</td><td>20</td><td>10</td><td>0</td></tr><tr><td>BX</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td><td>10</td></tr><tr><td>CX</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td></tr></table>	Working is expected by performing a dry run.	6
	e		Operation – Division. Final Value of AX is called the remainder.	1 mark for division 1 mark for remainder	2
				Total:	**20**
3	a	i	Address bus: Address number for memory location.		1
		ii	Data bus: Actual data being transferred/processed		1
		iii	Control bus: Carries control signals from CPU and returns status signals.		1
	b		The function of the system clock is to synchronise all of the operations of a computer.		2
	c		The CU and ALU are the main building blocks of a CPU. The ALU is responsible for performing both arithmetic and logic operations such as addition, subtraction etc. The Control Unit is responsible for decoding operations as well as directs all other operations of the processor.	2 2	4
	d		See figure below 	2 marks for bus names and widths. 1 mark for bus direction. 1 mark for drawing of CPU and main memory blocks. 2 marks for memory sizing	6

	e		Contents of Program Counter (PC) transferred to Memory Address Register (MAR). Value of MAR is transferred to Address Bus. PC is incremented. Fetch value or instruction from memory through data bus. Contents of addressed memory loaded into Memory Data Register (MDR). Transfer contents from MDR to Current Instruction Register.	1 mark for each correct step (ignoring PC is incremented)	5
				Total:		**20**
4	a		Lexical Analysis: Removal of redundant text. Error Handling. Conversion of Lexemes into tokens. Syntax and Semantic Analysis: Parsing. Symbol Table. Compile-time error detection and handling. Code optimisation and generation: Simple code optimisation techniques. Translation into object code. Linking.	2 marks for each stage	6
	b		A syntax error is invalid code that is not understood by the compiler. Example: Missing semicolon, unbalanced expressions etc. A semantic error is valid code that compiles but generates an error during runtime or undefined behaviour. Example: Incrementing a non-initialised variable	1 1 1 1	4
	c	i	`A B * C D - +`		2
		ii	`C - A / 5 * B D - /`		3
	d		`A/(B+C-D) = 5.` Note: Working is indicative. Students may use different methods as long as they clearly show the stack. 2 4 3 3 5 5 1 5 5 5 5 5 5 5 + - /	1 mark for correct infix answer 2 marks for correct answer 0 marks for answer only	5
				Total:		**20**

5	a		Device handshaking is a setup procedure, which will allow a peripheral to communicate with a computer. The peripheral would send some setup bits to the computer to set up a connection, and the computer would reply with an acceptance or decline message. Once both the connection is setup, both parties may start communicating.		4
	b		An online operating system would be best. This involves remotely accessing another computer through an internet browser. The user experience is as though the operating system is running on the physical machine s/he is actually using.	1 3	4
	c	i	round robin		2
		ii	Fair and each process gets a fixed timeslot. Processes, which require more time will take longer to be processed.	1 1	2
		iii	Another system is priority scheduling. Processes with highest priority will be run first. An advantage is that urgent jobs can be served quickly. This might lead to process starvation for low priority jobs.	1 1 1 1	4
	d		Software polling consists of the CPU continuously checking whether peripherals / devices need processing time. It is used in the context of I/O operations.		4
				Total:	**20**
6	a	i	full duplex		1
		ii	half duplex		1
		iii	simplex		1
	b		modulation can increase the speed of data transmission, as more signals can be transmitted over the same medium. Amplitude modulation, frequency modulation, phase modulation.	2 marks 1 mark each for any one	3
	c		Wifi WiFi uses the IEEE 802.11 standard, and consists of a wireless router which receives and transmits data from and to wireless devices. WiFi has a range of up to ~100 m and can support a high data rate. Bluetooth Bluetooth is meant for close range communication and supports lower data rate. It takes the form of a peer-to-peer network.	1 2 1 2	6
	d	i	Provides a reference model on which actual protocols are based.		2
		ii	Physical layer: the lowest layer of the OSI model. Its main function is to control how a bit-stream of data is sent and received over the physical medium. E.g. it must decide amongst others: what type of cable is being used for the connection; how many pins the connectors have and what each pin represents; which signal pattern will represent a binary 1; what voltages and currents are used. Data Link layer: provides low-level error detection and correction. For example if a packet is corrupted this layer is responsible for retransmitting the packet. The layers above this layer can assume	3 marks each for any two	6

			virtually error-free transmission over the network. This layer organizes the data as frames i.e. group of bits. For example it is in this layer that CRC is carried out on the data. Network layer: responsible for routing packets of data across the network and fragmenting large packets and reassembling them in the right order. Transport layer: responsible for end-to-end integrity and passing of the data. It is responsible for the correct delivery of data to the other end. Session layer: manages the "current" connection (or session) to the network. It handles such things as: opening of connection, sending and receiving data on connection, closing of connection. Presentation layer: ensures the end points speak the same language. This layer resolves any data encoding differences between the communicating nodes by translating to and from the code systems in use at each end. For example it may convert text to ASCII (American Standard Code for Information Interchange) or EBCDIC (Extended Binary Coded Decimal Interchange Code) form. Application layer: serves as a window (interface) for users and applications processes to access network services. It is the highest layer in the model and hides all the lower layers to the user.		
				Total:	**20**
7	a		<table><tr><th>Name</th><th>Address</th><th>Telephone No.</th><th>Movies rented</th></tr><tr><td>Joe Attard</td><td>3, Rock street, Lija</td><td>32903</td><td>Avengers</td></tr><tr><td>Joe Attard</td><td>3, Rock street, Lija</td><td>32903</td><td>Pirates of the Caribbean</td></tr><tr><td>Rose Borg</td><td>53, Orange Street, Qrendi</td><td>17930</td><td>Titanic</td></tr><tr><td>Martin Said</td><td>8, Flower Street, Sliema</td><td>89302</td><td>Midnight in Paris</td></tr><tr><td>Martin Said</td><td>8, Flower Street, Sliema</td><td>89302</td><td>The Lion King</td></tr><tr><td>Rose Borg</td><td>13, Fish Street, Bugibba</td><td>230231</td><td>Pokemon Detective Pikatchu</td></tr></table> <table><tr><th>ID</th><th>Name</th><th>Address</th><th>Telephone No.</th><th>Movies rented</th></tr><tr><td>1</td><td>Joe Attard</td><td>3, Rock street, Lija</td><td>32903</td><td>Avengers</td></tr><tr><td>1</td><td>Joe Attard</td><td>3, Rock street, Lija</td><td>32903</td><td>Pirates of the Caribbean</td></tr><tr><td>2</td><td>Rose Borg</td><td>53, Orange Street, Qrendi</td><td>17930</td><td>Titanic</td></tr></table>	4 marks for stating that entries need to be atomic, and therefore 1st NF would be 4 marks for stating that a unique ID is needed for 2nd NF would be	12

			3	Martin Said	8, Flower Street, Sliema	89302	Midnight in Paris
			3	Martin Said	8, Flower Street, Sliema	89302	The Lion King
			4	Rose Borg	13, Fish Street, Bugibba	230231	Pokemon Detective Pikatchu

ID	Name	Address	Telephone No.
1	Joe Attard	3, Rock street, Lija	32903
2	Rose Borg	53, Orange Street, Qrendi	17930
3	Martin Said	8, Flower Street, Sliema	89302
4	Rose Borg	13, Fish Street, Bugibba	230231

ID	Movies rented
1	Avengers
1	Pirates of the Caribbean
2	Titanic
3	Midnight in Paris
3	The Lion King
4	Pokemon Detective Pikatchu

4 marks for stating that 3rd NF would be

	b		Transitive dependencies are removed and data duplication is reduced. Data integrity is improved.	2 2	4
	c		Stating design, installation and configuration of database. Monitoring, backup and data recovery of database.	2 2	4
				Total:	**20**
8	a	i	Recursive programming.		2
		ii	Type of programming is simpler. May use more memory.	1 1	2
		iii	2 2 4 8 3 2 valid attempt but makes a mistake	4 marks for correct answer 2 marks for valid answer	4

	b	i	Inheritance allows a class to reuse functionality from the superclass. It is used in `programmer.getSalary()`	2 2	4
		ii	Yes Employee does not inherit from Programmer.	1 1	2
	c		Hash value is fully determined by the data being hashed. Hash function generates very different hash values for similar inputs. Uniformly distributes data across the entire set of possible hash values.	2 2 2	6
				Total:	**20**